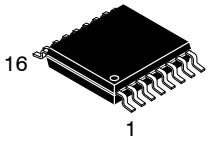
5S Battery Protector with State of Charge Indication

Advance Information

NCS35011



TSSOP−16
CASE 948F

The NCS35011 is an ultra−low power protection integrated circuit managing lithium−ion batteries from 3 to 5 cells in series with accurate battery voltage indication up to 5 LED outputs.

Each cell in the battery pack is monitored for an over−voltage and under−voltage condition. Upon detecting an over−voltage, the ODI pin will assert indicating a fault condition and stay asserted until the fault is cleared. During an under voltage condition, the UDI pin will also assert indicating the fault but will have a pulse width that is pre−set in the protector. Both over and under voltage detections have a hard coded pre−set delay time before fault indication.

Pulling the ENB high will start a measurement of the battery pack voltage which will be compared to a pre−set detection threshold table. If a threshold voltage is exceeded the protector will power the corresponding LED to indicate state of charge of the pack.

Hardware protection and battery monitoring run autonomously and allows operation without a microcontroller.

Features

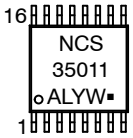
- Over−Voltage (OV) and Under−Voltage (UV) Detection
- Protection for 3, 4 and 5 Series Cells
- State of Charge (SoC) Indication with High Voltage Tolerant LED Drivers
- Configurable Fault Outputs (Active High or Low for Push−Pull or Open Drain)
- High−Accuracy Voltage Measurement ±5 mV
- Low Power Consumption I_{cc} = 4 μA
- Input BAT Voltage Range 5 V to 28 V, tolerant to 70 V for Increased Immunity to Surge
- Extended Junction Temperature Range to 125°C
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Secondary Protection
- Power and Gardening Tools
- Portable/Autonomous Equipment (Cleaners, Mowers, Motive, Medical)

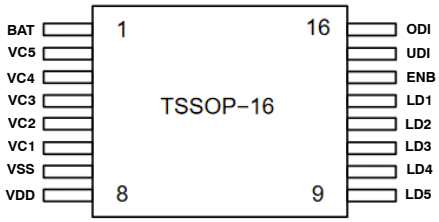
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MARKING DIAGRAM



NCS35011 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCS35011DTBR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Block Diagram

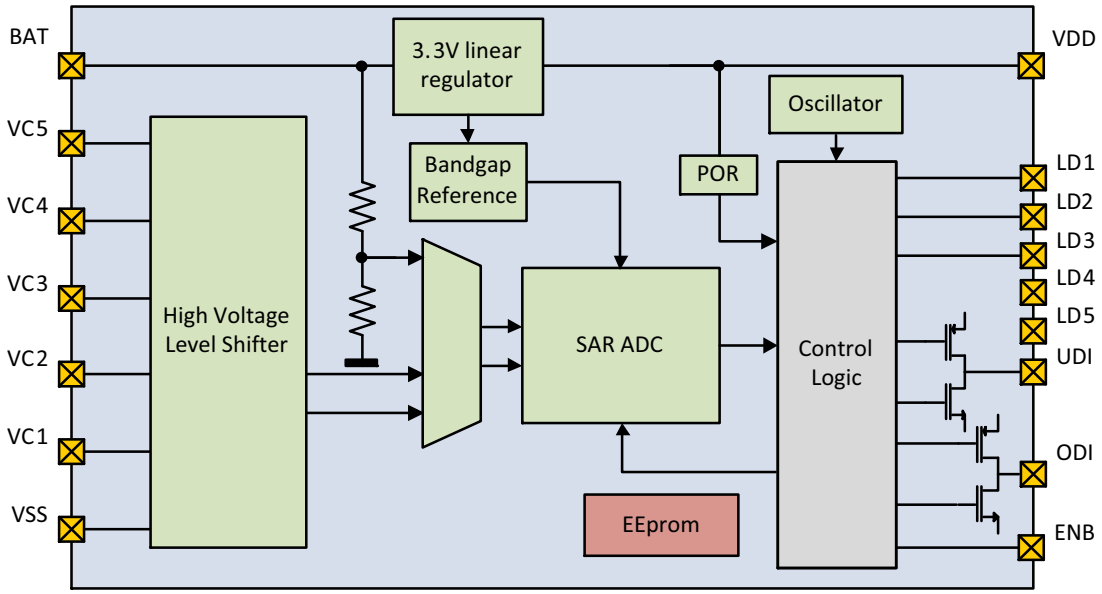


Figure 1. Simplified Block Diagram

Pin Connections

TSSOP−16

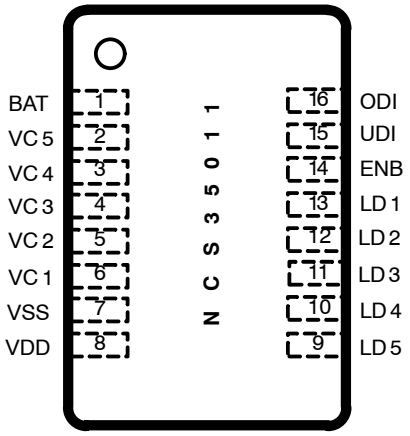


Figure 2. NCS35011 Pinout (TSSOP−16)

PIN DESCRIPTION

Signal Name	Pin No.	Type	Description
BAT	1	Power	Positive Battery input voltage
VC5	2	Analog	Battery cell 5 voltage
VC4	3	Analog	Battery cell 4 voltage
VC3	4	Analog	Battery cell 3 voltage
VC2	5	Analog	Battery cell 2 voltage
VC1	6	Analog	Battery cell 1 voltage
VSS	7	Ground	Negative Battery input voltage
VDD	8	Power	3.3 V regulator output voltage
LD5	9	Output Open Drain	LED output 5, open drain; active low

PIN DESCRIPTION (continued)

Signal Name	Pin No.	Type	Description
LD4	10	Output Open Drain	LED output 4, open drain; active low
LD3	11	Output Open Drain	LED output 3, open drain; active low
LD2	12	Output Open Drain	LED output 2, open drain; active low
LD1	13	Output Open Drain	LED output 1, open drain; active low
ENB	14	Input	LED output indication enable input; pull down, active high
UDI	15	Output	Cell Under voltage detection output indication; configurable (CMOS active low or high; nFET open drain active on or off)
ODI	16	Output	Cell over voltage detection output indication; configurable (CMOS active low or high; nFET open drain active on or off)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input voltage (Note 1)	V_{BAT}	−0.5 to 70	V
Supply Current	I_{BAT}	10	mA
VC1, VC2, VC3, VC4, VC5, ODI, UDI, LD1, LD2, LD3, LD4, LD5 voltage	V_{IHV}	−0.5 to 70	V
ENB, NC voltage	V_{ILV}	V_{BAT}	V
VCn − VCn−1 differential cell input voltages	V_{CELLD}	−0.5 to 30	V
Maximum Junction Temperature	$T_{J(max)}$	125	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Charge Device Model (Note 2)	ESD_{CDM}	500	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, TSSOP−16 (Note 1) Thermal Resistance, Junction−to−Air (Note 5) Thermal Reference, Junction−to−Case (Note 5)	 $R_{\theta JA}$ $R_{\psi JC}$	115	°C/W

4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Typ	Max	Unit
BAT Input voltage	V_{BAT}	5	18	28	V
Cell voltage (VC1, VC2, VC3, VC4, VC5)	V_{CELL}	2		5	V
ODI, UDI voltage	V_{PRES}	0		V_{BAT}	V
LED voltage (LD1, LD2, LD3, LD4, LD5)	V_{LED}	0		V_{BAT}	V
ENB voltage	V_{EN}	0		V_{BAT}	V
Ambient Temperature	T_A	−40		85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL SPECIFICATIONS

Rating	Symbol	Min	Typ	Max	Unit
VOLTAGE MONITORING (VC1, VC2, VC3, VC4, VC5 and BAT)					
BAT Voltage Detection Accuracy (T_A = 25°C)	V_{BAT_QA}		<75		mV
Cell Voltage Detection Accuracy (T_A = 25°C, VCx = 3V to 4.7V)	V_{OA}	−5		5	mV
Cell Voltage Detection Accuracy Across Temperature (T_A = −40 to 85°C)	V_{OAD}	−30		30	mV
Overvoltage Detection (OVD) Range (Note 5)	V_{OVD}	3.6		4.7	V
Overvoltage Detection Hysteresis (OVH) Range (Note 5)	V_{OVH}	50		500	mV
Undervoltage Detection (UVD) Range (Note 5)	V_{UVD}	1.5		2.8	V
Undervoltage Detection Hysteresis (UVH) Range (Note 5)	V_{UVH}	50		500	mV
BAT Voltage to Active LD1 Pin for SoC Indication	V_{DET1}		Table 2		V
BAT Voltage to Active LD1−2 Pin for SoC Indication	V_{DET2}		Table 2		V
BAT Voltage to Active LD1−3 Pin for SoC Indication	V_{DET3}		Table 2		V
BAT Voltage to Active LD1−4 Pin for SoC Indication	V_{DET4}		Table 2		V
BAT Voltage to Active LD1−5 Pin for SoC Indication	V_{DET5}		Table 2		V
SUPPLY AND LEAKAGE CURRENT					
Supply Current − Standby mode with no fault and ENB low	I_{CC}		4		μA
Input Current at VCx pins	I_{IN}	−0.1		0.1	μA
Supply Current − State of Charge Mode (ENB=3.6V,LDx=0,VCx=4V, T_A = 25°C)	I_{SOC}		26		μA
ODI/UDI OUTPUT PIN, CMOS ACTIVE HIGH OR LOW VERSION					
ODI/UDI Active High Across Temperature ($I_{ODI-H} \le$ 5 mA, *Tested with V_{BAT}=5V)	V_{ODI-H}		*V_{BAT}−1.7		V
ODI/UDI Active Low Across Temperature ($I_{ODI-L} \le$ 5 mA)	V_{ODI-L}		0.1		V
OUTPUT DRIVE ODI/UDI, OPEN DRAIN NMOS FET ACTIVE ON OR OFF VERSION					
Static Drain−Source On−Resistance (nFET On−Resist), I_{ODI} = 5mA, T_A = 110°C	R_{DS-ON}			15	Ω
ODI/UDI Off Current	$I_{ODI-OFF}$			0.1	μA
ENB INPUT					
ENB Input Voltage “High”	V_{EN-H}		1.5		V
ENB Input Voltage “Low”	V_{EN-L}		1.3		V
ENB Pull Down Current	I_{PD}		50		kΩ
LED OUTPUT CURRENT DRIVE					
Output Sink Current	I_{LED-ON}			10	mA
Output Leakage Current	$I_{LED-OFF}$			0.1	μA

TIMING REQUIREMENTS

Rating	Symbol	Min	Typ	Max	Unit
DELAY TIMER					
Overvoltage Delay Time (ODEL) Configuration Range (Note 5)	t_{ODEL}	0.94	Table 3	5	s
Undervoltage Delay Time (UDEL) Configuration Range (Note 5)	t_{UDEL}	0.125	Table 3	1	s
Undervoltage Pulse Time (UPUL) Configuration Range (Note 5)	t_{UPUL}	1	Table 3	5	s
Delay/pulse Response Timing Accuracy (T_A = 25°C)	t_{error}	−6%		6%	
Delay/pulse Response Timing Accuracy Across Temperature (T_A = −40 to 85°C)	t_{error}		6%		
DEBOUNCE/DUTY CYCLE					
ENB Debounce for SoC Indication (Note 5)	t_{ENB}	30		55	ms
LDx Pulse Duration (LEDD) Time Configuration Range (Note 5)	t_{LEDD}	0.05	Table 3	5	s

5. These configurations are programmed at the factory, they are not customer programmable. However, for high volumes, **onsemi** can define further IC variants with any combination of the shown configurations NCS35011DBxyR2G. Contact your sales representative.

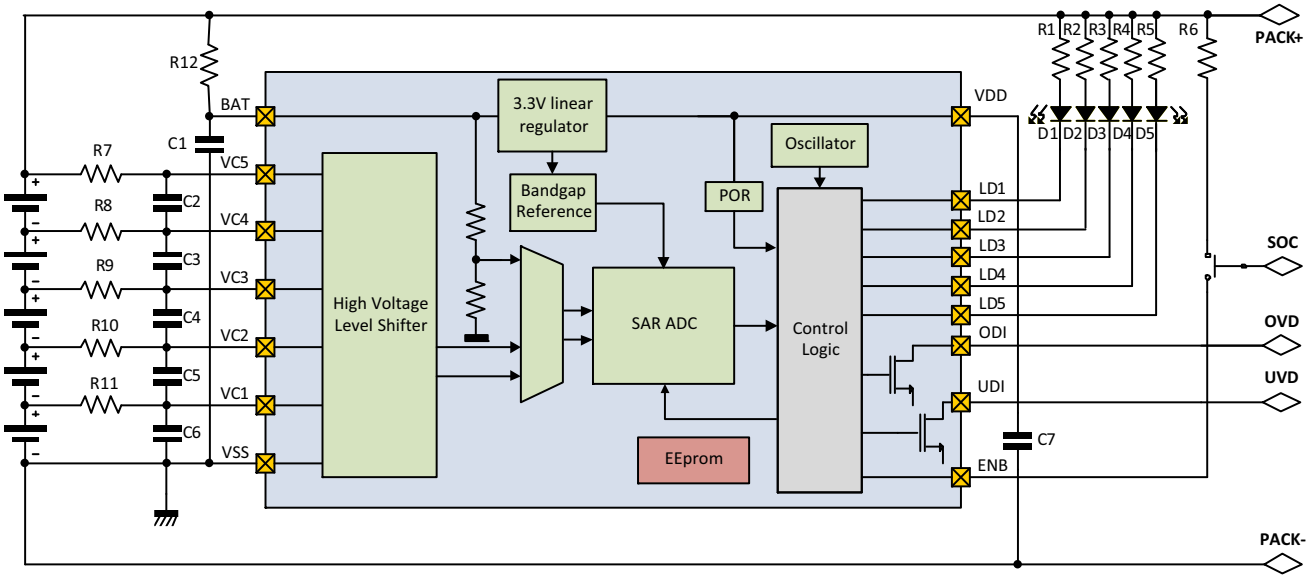


Figure 3. 5S Battery Pack, 5 LEDs, Open Drain Outputs Application Diagram

Table 1. RECOMMENDED EXTERNAL COMPONENTS

Component Type	Instance	Value	Note
LED	D1,D2,D3,D4,D5	–	LEDs for state of charge indication
Capacitor	C1	1 μF	Battery pack voltage capacitor
Capacitor	C2,C3,C4,C5,C6	100 nF	Input cell voltage filter capacitor
Capacitor	C7	1 μF	3.3V regulator output filter capacitor
Resistor	R1,R2,R3,R4,R5	4.7 kΩ	LED current limiting resistor, set according to desired brightness; To guarantee the chip spec, it is recommended to limit each LED current less 10 mA.
Resistor	R6	1 kΩ	Limiting resistor for switch input refer to ENB pull−down current spec to set the resistance
Resistor	R7,R8,R9,R10,R11	1 kΩ	Input cell voltage filter resistor
Resistor	R12	1 kΩ	Battery input filter resistor; Limit R12 resistance when IC ODI/UDI pin is configured as CMOS push/pull (Note 6)

6. All VC pin internal high side ESD diodes are connected to BAT pin for ESD protection purpose. When ODI/UDI pin is driving a resistive load and consume a large current through BAT pin, a large IR drop through R12 may result VC5 pin voltage higher than BAT pin and forward bias VC5 pin internal high side ESD diode.

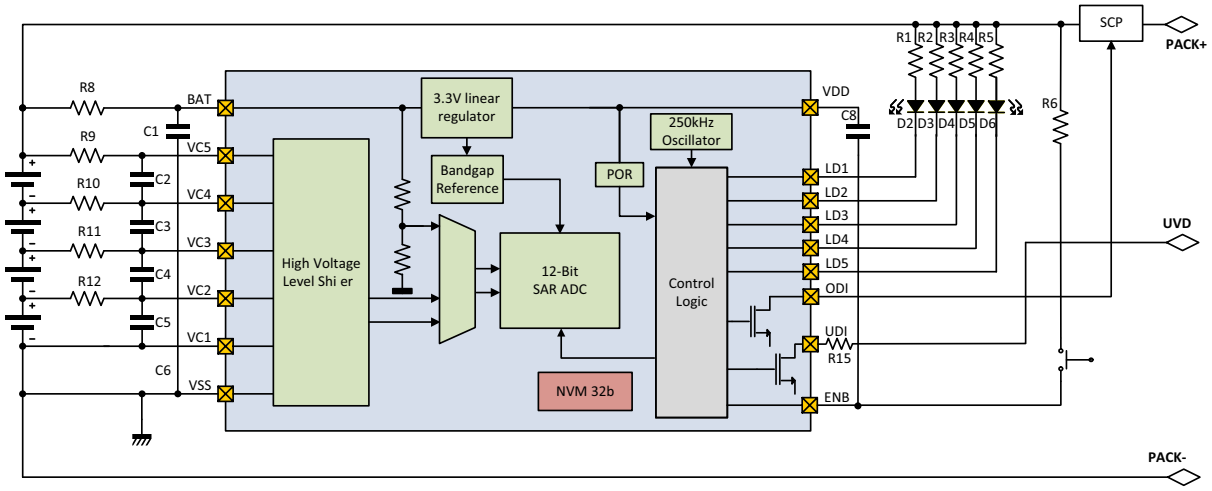


Figure 4. 4S Battery Pack, 5 LEDs, Open Drain Outputs with SCP Application Diagram

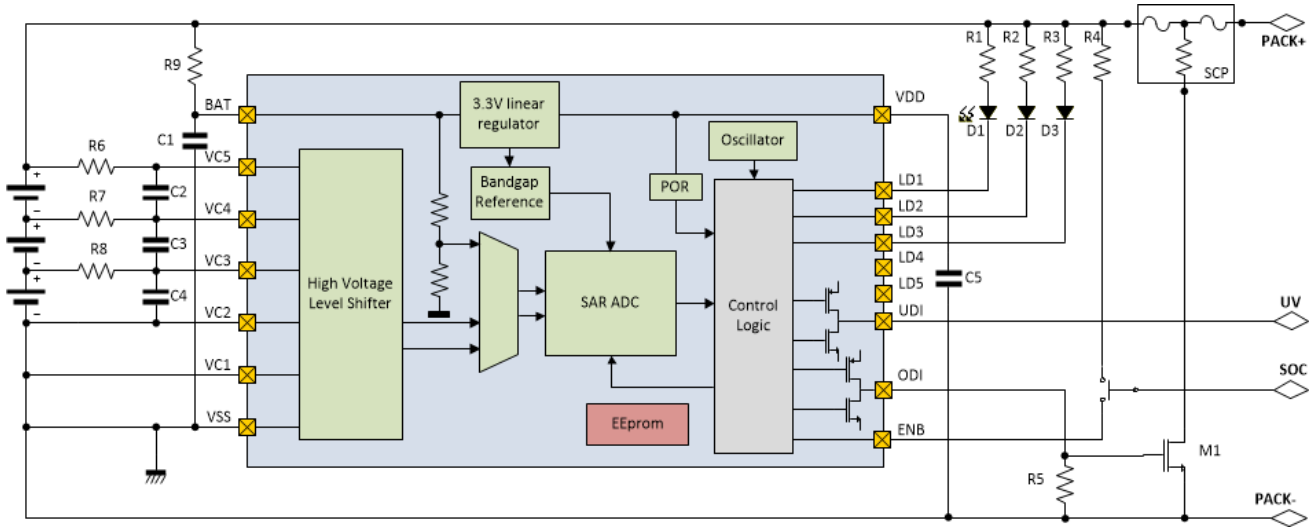


Figure 5. 3S Battery Pack, 3 LEDs, Push−Pull Outputs with SCP Application Diagram
Note: Having series resistor on VC2 and VC1 will help with system level ESD

Detailed Description

The NCS35011 is an individual cell−monitoring device that checks for over and under voltage conditions in 3 to 5S battery packs. Figure 3−5 shows the 3, 4, and 5 series of battery pack application diagram, and the IC expect VC1/VC2 to be grounded in 3S and VC1 to be grounded in 4S application. The device also monitors the pack voltage and drives LEDs that indicate the voltage level for a rudimentary state of charge indication.

Overvoltage and Under−voltage Detection

Monitoring for an overvoltage condition occurs by comparing each cell voltage (VCx) with a predetermined threshold set by the parameter V_{OV}. An on−chip ADC samples each cell voltages every 125 ms, so this can affect the overvoltage and under−voltage response time. If any cell voltage goes above the V_{OV} threshold for the predetermined t_{DEL-OV} time limit, the IC will actuate the ODI pin depending on the pin configuration to indicate a fault. If all of the individual cell voltages drop back down below the V_{OV} threshold, the ODI pin will default back to the normal operational state. ODI pin will either pull low internally (recommend to limit this current less than 5 mA), if configured as nFET active low, or will be pulled high through external pull−up resistor, if configured as nFET active high impedance; ODI pin can also be configured as CMOS active low or high.

Under−voltage detection occurs by comparing each cell voltage (VCx) with a predetermined threshold set by the parameter V_{UV}. If any cell voltage goes below the V_{UV} threshold for the t_{DEL-UV} time limit, the IC will assert the UDI pin to indicate a fault. A fault indication will assert the UDI pin for the time duration specified by the parameter t_{ON-UV}. A cell voltage recovery back to a normal level will not interrupt the UDI signaling. To detect a new under−voltage fault condition all cell voltages will need to return to a normal level and then drop below the V_{UV} threshold for the specified delay time $t_{DEL-UV.}$ UDI pin will either pull low internally (recommend to limit this current less than 5mA), if configured as nFET active low, or will be pulled high through external pull−up resistor, if configured as nFET active high impedance; UDI pin can also be configured as CMOS active low or high.

Figure 6 shows timing waveforms of the overvoltage and under−voltage fault detection. Table 1 lists key parameters for each of the fault conditions.

Battery Pack Voltage State of Charge Indication

When the ENB pin asserts high for the time limit set by t_{ENB} the NCS37011 will measure the voltage at the BAT pin and compare it to the thresholds set by $V_{DETX.}$ If the detection level exceeds the predetermined threshold, the appropriate LDx open drain pulldown will assert turning on the corresponding LED for the time duration $t_{PUL-LED}$ and then shut off. To restart the LEDs the ENB pin will assert low for the time limit t_{ENB} and then assert high again for the same amount of time. Figure 6 shows the ENB input timing waveform for state of charge indication.

NCS37011 has 4 multiplier sets to choose from, shown in Table 2. The threshold voltage for different LED pin to turn on are dependent upon number of cells (VC_COUNT) in the battery pack and the configured over voltage (OVD) per cell. Each LED threshold is set by multiplying a constant (Multiplier) times the product of VC_COUNT and OVD. This creates the typical threshold $V_{DETX.}$

Product = VC_COUNT * OVD;

V_{DETX} = Product * Multiplier.

Table 2.

SoC Multiplier Sets	LED pin (LDx)	Symbol (V_{DETX})	Multiplier
A	LD5	V_{DET5}	0.954
	LD4	V_{DET4}	0.936
	LD3	V_{DET3}	0.898
	LD2	V_{DET2}	0.837
	LD1	V_{DET1}	0.585
B	LD5	V_{DET5}	0.918
	LD4	V_{DET4}	0.875
	LD3	V_{DET3}	0.847
	LD2	V_{DET2}	0.819
	LD1	V_{DET1}	0.781
C	LD5	V_{DET5}	0.877
	LD4	V_{DET4}	0.847
	LD3	V_{DET3}	0.788
	LD2	V_{DET2}	0.765
	LD1	V_{DET1}	0.729

Table 2.

SoC Multiplier Sets	LED pin (LDx)	Symbol (V_{DETX})	Multiplier
D	LD5	V_{DET5}	0.931
	LD4	V_{DET4}	0.883
	LD3	V_{DET3}	0.841
	LD2	V_{DET2}	0.756
	LD1	V_{DET1}	0.659

NOTE: Depends on the application, user may combine or skip certain LED pins to create a desired SoC combination. Unused LED pin can be floated.

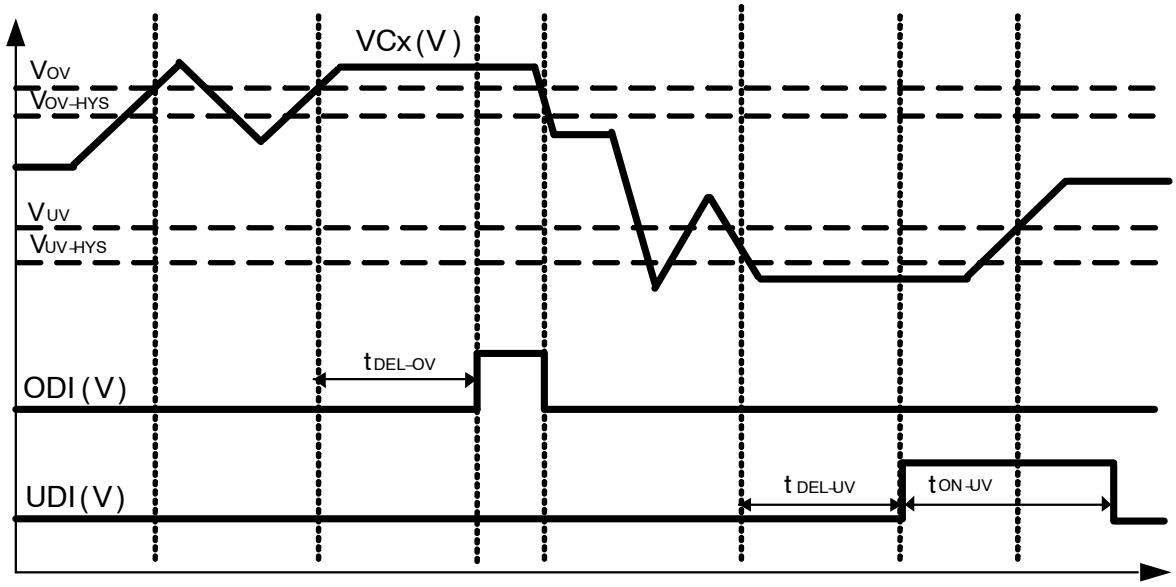


Figure 6. Timing for OV and UV Detection

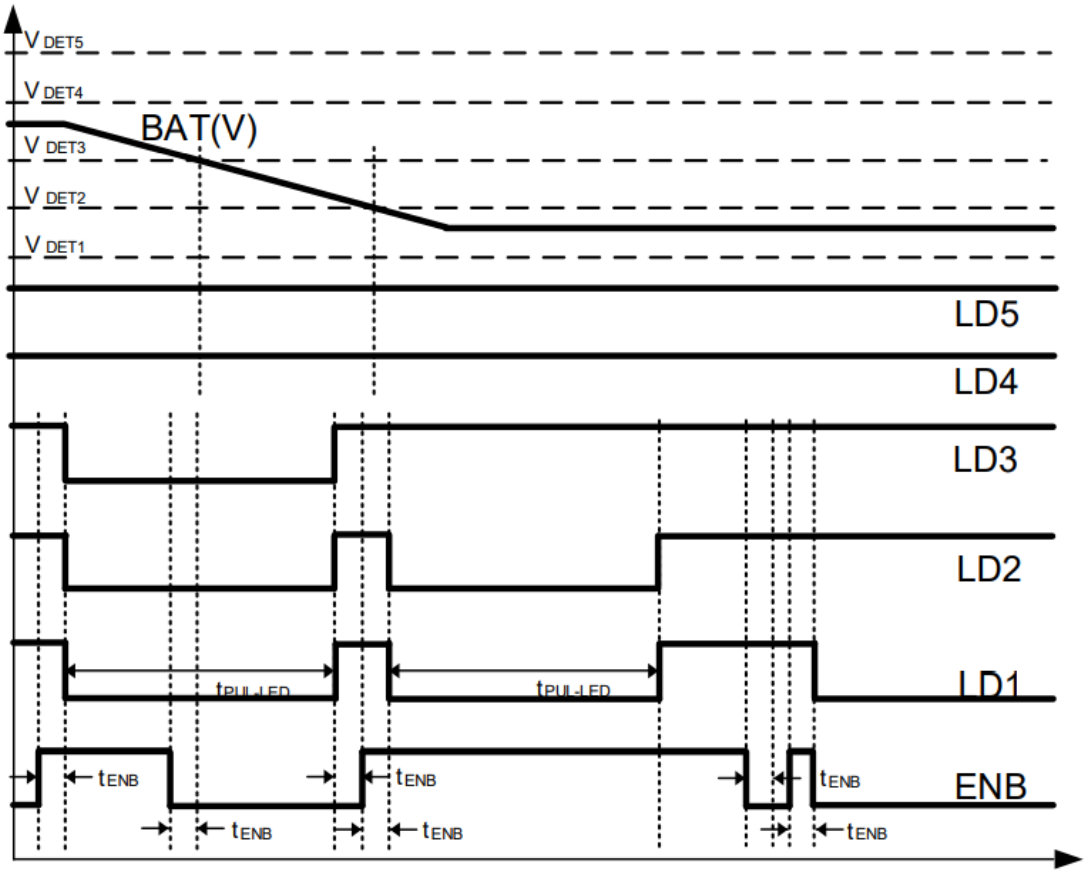


Figure 7. ENB Input Timing for State of Charge Indication

Table 3. ORDERABLE PART DIFFERENTIATION

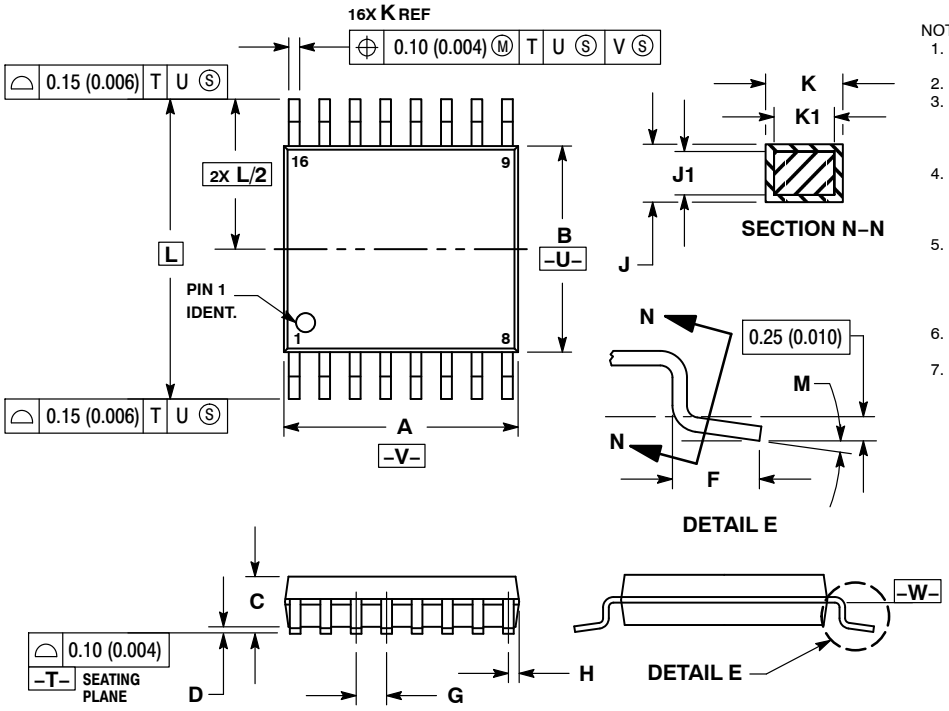
Part Number	3/4/5 S	OVD (V)	OVH (V)	UVD (V)	UVH (V)	ODEL (s)	UDEL (s)	UPUL (s)	OV Output	OV Polarity	UV Output	UV Polarity	LEDD (s)	SoC sets
NCS35011D-TBR2G	5	4.275	0.05	2	0.25	0.94	1	1.5	OD	1	OD	0	3	A
NCS35011D-TBxyR2G	3−5	3.6−4.7	0.05 −0.5	1.5−2.8	0.05 −0.5	0.94−4.94	0.125 −1	1−5	OD/PP	0/1	OD/PP	0/1	0/3/5	A/B/C/D

NOTE: **OD** = nFET open drain; **PP** = CMOS push or pull;
nFET open drain (OV/UV polarity 0): active low (nFET ON);
nFET open drain (OV/UV polarity 1): active high impedance (nFET OFF);
CMOS push−pull (OV/UV polarity 0): active low;
CMOS push−pull (OV/UV polarity 1): active high;

For high volumes, **onsemi** can define further IC variants with any combination of the shown configurations NCS35011DTBxyR2G. Contact your sales representative.

PACKAGE DIMENSIONS

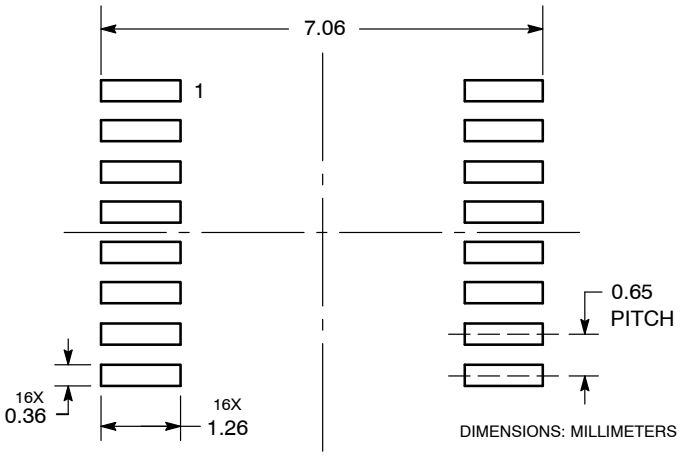
TSSOP−16
CASE 948F
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



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