High Voltage, High Current Darlington Transistor Arrays

ULN2003A, ULQ2003A

The seven NPN Darlington connected transistors in these arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to 500 mA permit them to drive incandescent lamps.

The ULx2003A with a 2.7 kΩ series input resistor is well suited for systems utilizing a 5.0 V TTL or CMOS Logic.

Features

- These are Pb-Free Devices

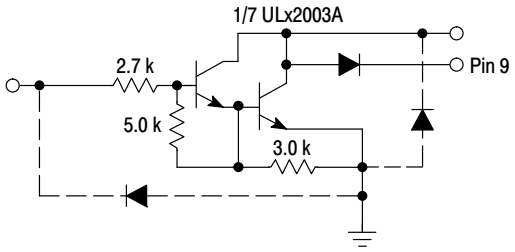
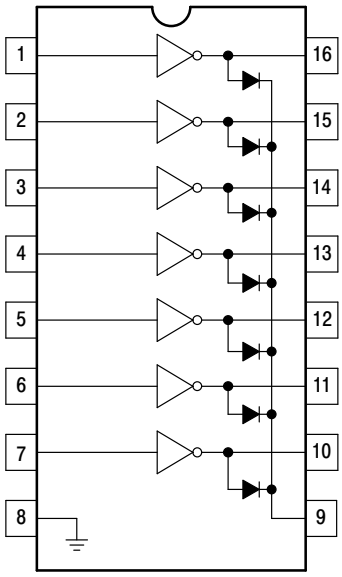
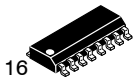


Figure 1. Representative Schematic Diagram



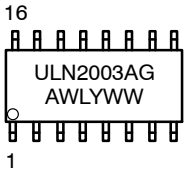
(Top View)

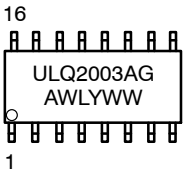
Figure 2. Pin Connections



SOIC-16
D SUFFIX
CASE 751B

MARKING DIAGRAMS





A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
ULN2003ADR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
ULQ2003ADR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS (T_A = 25 °C, and rating apply to any one device in the package, unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage	V_I	30	V
Collector Current - Continuous	I_C	500	mA
Base Current - Continuous	I_B	25	mA
Operating Ambient Temperature Range ULN2003A ULQ2003A	T_A	 −20 to +85 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	150	°C
Thermal Resistance, Junction-to-Ambient Case 751B, D Suffix	$R_{\theta JA}$	 100	°C/W
Thermal Resistance, Junction-to-Case Case 751B, D Suffix	$R_{\theta JC}$	 20	°C/W
Electrostatic Discharge Sensitivity (ESD) Human Body Model (HBM) Machine Model (MM) Charged Device Model (CDM)	ESD	 2000 400 1500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Leakage Current	I_{CEX}				μA
(V_O = 50 V, T_A = +85 °C)		–	–	100	
(V_O = 50 V, T_A = +25 °C)		–	–	50	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 μA)		–	1.1	1.6	
(I_C = 200 mA, I_B = 350 μA)		–	0.95	1.3	
(I_C = 100 mA, I_B = 250 μA)		–	0.85	1.1	
Input Current - On Condition	$I_{I(on)}$				mA
(V_I = 3.85 V)		–	0.93	1.35	
Input Voltage - On Condition	$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 200 mA)		–	–	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)		–	–	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)		–	–	3.0	
Input Current - Off Condition	$I_{I(off)}$	50	100	–	μA
(I_C = 500 μA, T_A = 85 °C)					
DC Current Gain	h_{FE}	1000	–	–	–
(V_{CE} = 2.0 V, I_C = 350 mA)					
Input Capacitance	C_I	–	15	30	pF
Turn-On Delay Time	t_{on}	–	0.25	1.0	μs
(50% E_I to 50% E_O)					
Turn-Off Delay Time	t_{off}	–	0.25	1.0	μs
(50% E_I to 50% E_O)					
Clamp Diode Leakage Current T_A = +25 °C	I_R	–	–	50	μA
(V_R = 50 V) T_A = +85 °C		–	–	100	
Clamp Diode Forward Voltage	V_F	–	1.5	2.0	V
(I_F = 350 mA)					

TYPICAL PERFORMANCE CURVES - T_A = 25 °C

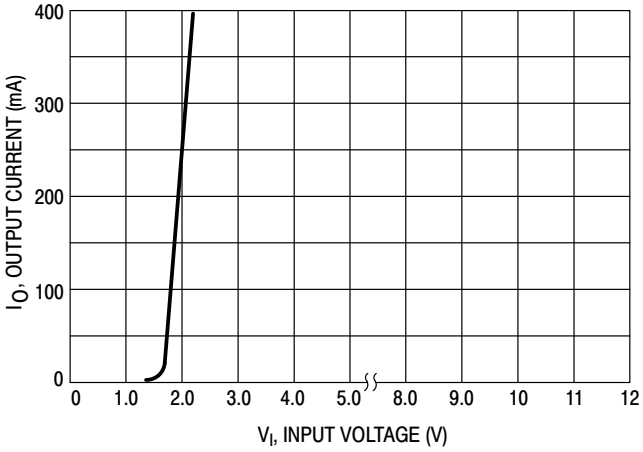


Figure 3. Output Current versus Input Voltage

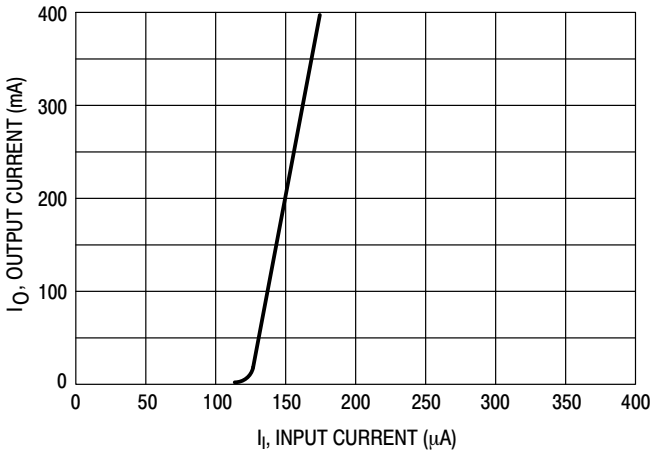


Figure 4. Output Current versus Input Current

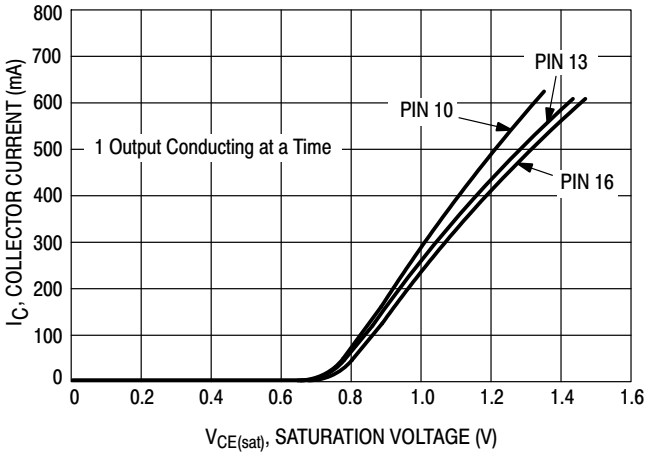


Figure 5. Typical Output Characteristics

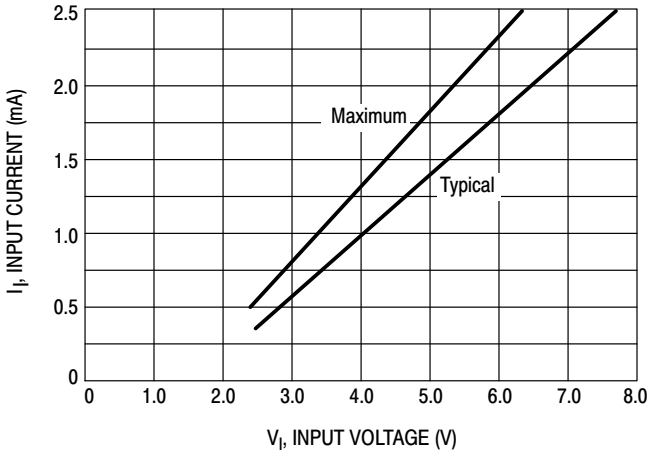


Figure 6. Input Characteristics

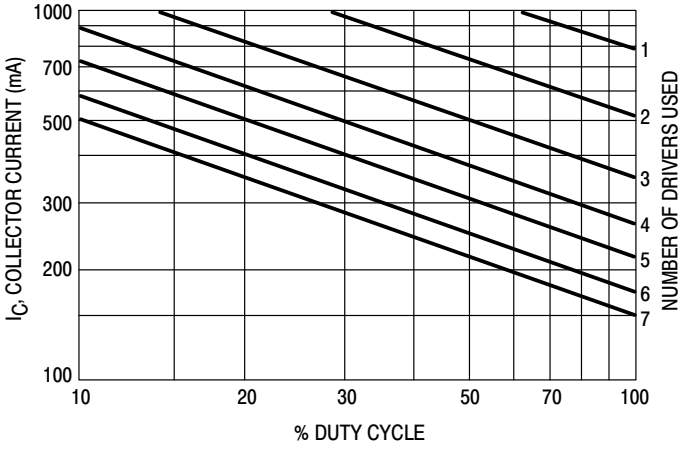
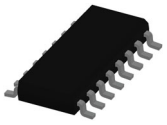


Figure 7. Maximum Collector Current versus Duty Cycle (and Number of Drivers in Use)

REVISION HISTORY

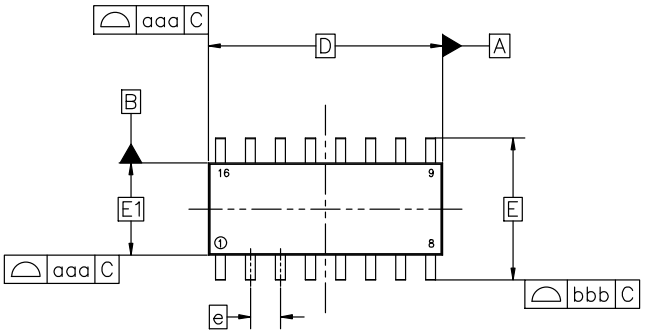
Revision	Description of Changes	Date
1	Rebranded the Data Sheet to **onsemi** format.	6/3/2025



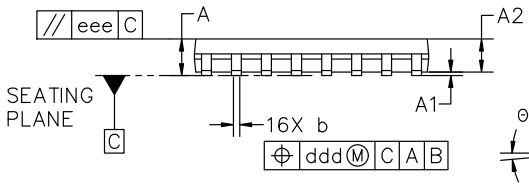
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

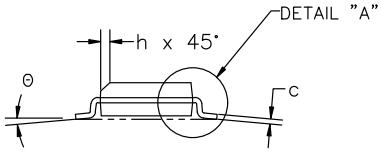
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



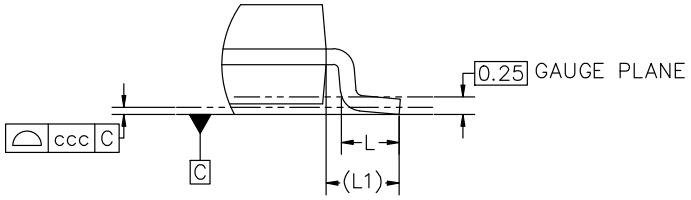
TOP VIEW



SIDE VIEW

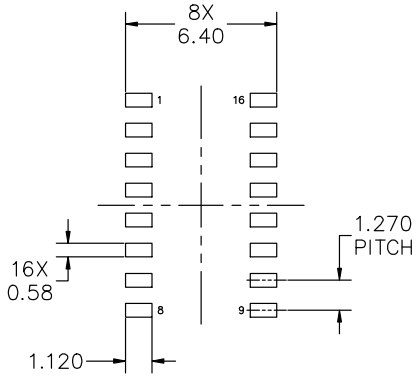


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

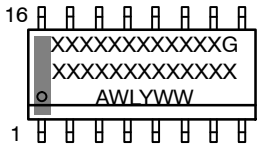
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

ADDITIONAL INFORMATION

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