Technical Reference Note

Embedded Power for
Business-Critical Continuity

VRM11.1
110 Amp

Total Power: 170 Watts
Input Voltage: 6.0 - 13.8 V
No. of Outputs: Single

RoHS 2002/95/EC

Special Features

- Vertical, horizontal, card edge, surface mount voltage regulator module
- Output current monitor
- Over-current protection
- Over-voltage protection
- Thermal warning
- Interleaved non-isolated multi-phase buck converter
- 8-bit voltage identification
- EU directive 2002/95/EC compliant for RoHS
- Dynamic VID
- PSI#, (Phase shedding)
- Remote sense
- Power good
- Output enable
- VRM11.1 compliant

Family Series: **VRM11.1 Series**
Function: **Single In-Line Power**
Usage: **Microprocessor, LEDs, ASIC, Memory, FPGAs, Telecom and Networking equipment, Servers, Industrial Equipment, POL Regulation**

Definition:

The VRM11.1 is a new high power density open frame non-isolated converter series for space-sensitive applications. Each model has a wide input voltage range (6.0 - 13.8 V) and offers a wide 0.5 - 1.6 V (at the output) with 8-bit voltage identification up to 110 A. The VRM11.1 has positive logic enable and over-current, over-voltage, and over temperature protection as standard. The output voltage is identified by VID code. VID code is provided by the microprocessor to the VRM11.1 which determines the reference output voltage. The VRM11.1 controller supports one 8-bit VRM11.0 linear table ranging from 0.03125 to 1.6 V (usable range of 0.5 - 1.6 V). The VRM offers a standard 0.8 mohm load impedance which can adjusted upon customer request. All features and functions of the VRM11.1 are designed according to Intel VRM and EVRD11.1 design guidelines.

Safety

Designed to meet:

- UL, cUL 60950-1
- (EN60950)

EMERSON
Network Power

General Description

Electrical Description

The VRM11.1 is implemented using a multi-phase, interleaved, synchronous buck topology. A block diagram of the converter is shown in Figure 1. The architecture reduces input and output ripple currents. Lower ripple current results in few components, lower costs, reduced power dissipation, and smaller implementation area.

The VRM11.1 meets the microprocessor's extremely fast edge rate transient (300 A/µs) by implementing Active Pulse Positioning (APP) and phase alignment APA modulation schemes. These implementations require fewer output capacitors and high efficiency from light to full load. The VRM11.1 achieves excellent light load efficiency by implementing phase shedding which allows the module to operate in one phase by grounding the PSI# Pin. During one phase mode, the module also offers excellent transient response.

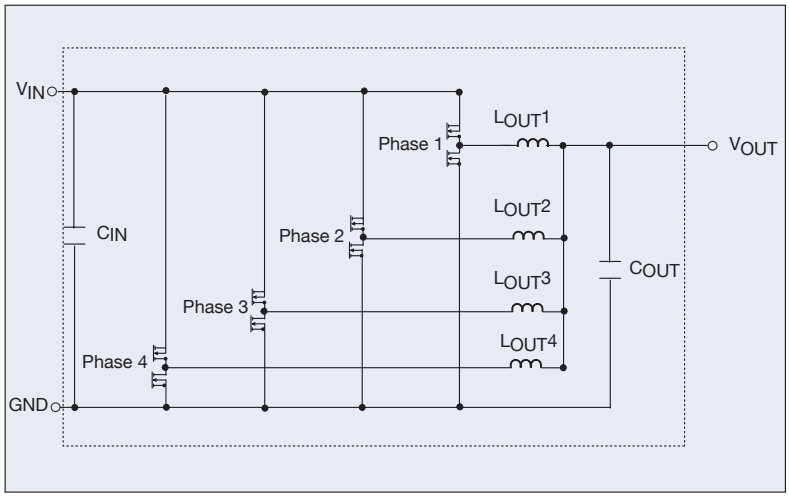


Figure 1 - Electrical Block Diagram

The VRM11.1 VR_READY signal offered by the VRM11.1 is pulled high to indicate that soft start has completed and the output voltage is within the regulated range around the VID setting. It is an open drain logic output. In the case of overcurrent or overvoltage, VR_READY will be pulled low. It will also be pulled low if the output voltage is below the undervoltage threshold.

The VRM11.1 VR_HOT Pin sends an advanced thermal warning, it will be pulled low when the VRM inductor core temperature is just above 100 °C. At this condition, the CPU should reduce its power consumption. The VR_HOT signal may be tied tot he CPU's PROC_HOT signal. For standard application drawing, see Figure 2.

The VRM11.1 is enabled by pulling the enable Pin high and disabled by leaving it floating or by connecting it to ground.

The output is adjustable over a range of 0.5 - 1.6 V by using the 8-VID control. Output is monitored for overcurrent and short-circuit conditions. When the PWM controller detects an overcurrent condition, it forces the module into hiccup mode.

Features

Output Voltage Adjustment
The output voltage on all models is adjustable from 0.5 - 1.6 V using 8-bit VID control. See Table 1.

Output Voltage Droop
The output voltage droop is set internally. The droop level depends on the required load line impedance.

Input Undervoltage Lockout
The VRM11.1 has a built in input undervoltage protection. Hysteresis determines when the module starts and turns off. The hysteresis levels depend on the input voltage operating range.

Output Overvoltage Protection (OVP)
The VRM11.1 protects the microprocessor load when over voltage occurs. The OVP trip point is the DAC setting plus 175 mV. The unit latches when overvoltage condition is detected and can only restart by recycling the input or the Enable Pin.

Over Current and Short-Circuit Protection
The VRM11.1 has two levels of over current protection (OCP). One is set by choosing the proper values for the I_{MON} Pin resistor. The voltage at I_{MON} Pin is proportional to load current, which is equal to 0.9 V at I_{MAX}. The I_{OCP} is triggered when V_{MON} = 1.11 V. Therefore, the over current proctection limit is: $I_{OCP} = 1.23\ I_{PEAK}$.

The second OCP limit is set usually higher than the first one. It is set internally and is proportional to the load current. When OCP occurs the unit transitions to hiccup mode and will return to normal operation conditions when the over current or short circuit no longer exists.

Over temperature Protection (OTP)
The VRM11.1 is equipped with non-latching over temperature protection. A temperature sensor monitors the temperature of the one phase core inductor. If the temperature exceeds a threshold of 115 °C the converter will shut down, disabling the output. When the temperature has decreased by 20 °C the converter will automatically restart.

Features

Wide Operating Temperature Range

The VRM11.1's ability to accommodate a wide range of ambient temperatures is the result of its high power conversion efficiency and resultant low power dissipation, combined with the excellent thermal performance of the PCB substrate. The maximum output power that the module can deliver depends on a number of parameters, primarily:

- Input voltage range
- Output load current
- Air velocity (forced or natural convection)
- Mounting orientation of target application PCB, i.e., vertical/horizontal mount, or mechanically tied down (especially important in natural convection conditions).
- Target application PCB design, especially ground planes. These can be effective heatsinks for the converter.

The VRM11.1 module has an operating temperature range of 0 °C to 70 °C with suitable derating and/or forced air cooling. Proper VRM11.1 operation is guaranteed if appropriate output power derating is applied. See Figure 3.

Pin Functions

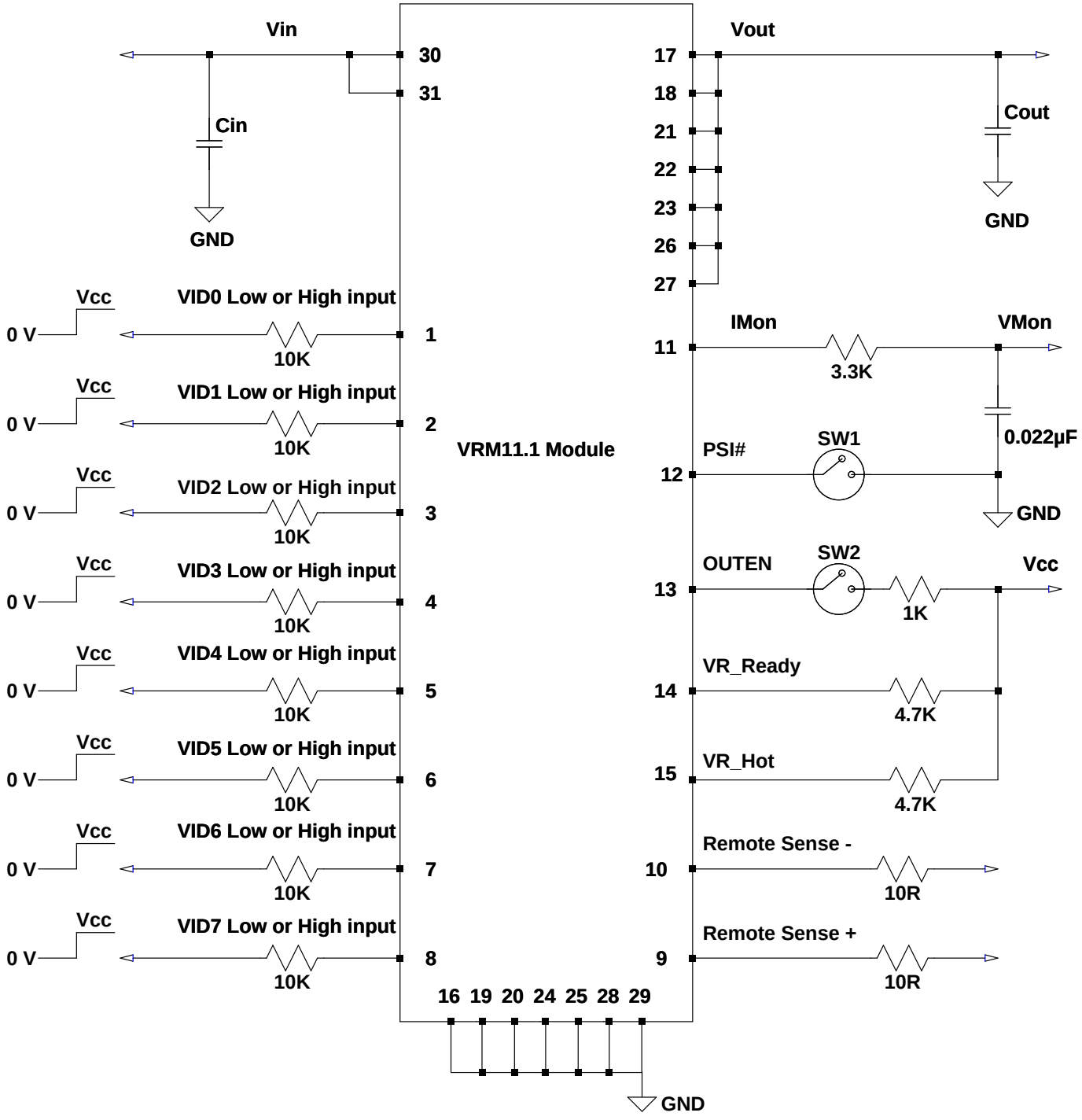


Figure 2 - Stamdard Application Drawing

Pin Functions (See Figure 2)

VID0 through VID7 - Pin 1-8

The standard VRM11.1 8-bit application. Output voltage can be set per the following VID table. VIDs are determined by the microprocessor and executed by the VRM11.1

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375

Pin Functions (cont'd)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375

Pin Functions (cont'd)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375

Pin Functions (cont'd)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375

Pin Functions (cont'd)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375

Pin Functions (cont'd)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

Pin Functions (cont'd)

Remote Sense(+) and Remote Sense(-) - Pins 9 and 10
The remote sense compensation feature minimizes the effect of resistance in the distribution system and facilitates accurate voltage regulation at the load terminals or another selected point. The remote sense lines will carry very little current and do not require a large cross-sectional area. However, if the sense lines are routed on a PCB, they should be located close to a ground plane in order to minimize any noise coupled onto the lines that might impair control loop stability. Remember that when using remote sense compensation all the resistance, parasitic inductance and capacitance of the distribution system are incorporated into the feedback loop of the power module. This can have an effect on the modules compensation capabilities, affecting its stability and dynamic response. Remote Sense(+) and Remote Sense(-) should run differential and in close proximity to each other, reaching the POL location through 100 ohm (maximum) in the system board.

I_{MON} - Pin 11
At the IMON Pin, a dc voltage can be read which is proportional to load current. To obtain an accurate current reading, connect an RC Low Pass Filter, R = 3.3 K and C= 0.022 uF, between IMON and GND. IMON voltage Pin is clamped to 1.11 V which indicates an overcurrent condition. The unit will shut down and go into hiccup mode. The VRM11.1 will resume normal operation when the load current is reduced. This is a buffered control indicator, external changes to this pin will not affect its operation.

PSI# Mode - Pin 12
At light load condition, $I_{LOAD} \leq 20$ A, the microprocessor should be able to connect the PSI# Pin to GND. When PSI# is grounded, the VRM11.1 module will shut down three phases to operate in a single phase mode. As a result the efficiency at light load condition is significantly improved.

Output Enable (OUTEN) - Pin 13
The Enable input allows external circuitry to put the VRM11.1 converter into a low dissipation standby mode. Positive logic is standard.

The unit is turned on if the Enable Pin is pulled high with a pull-up resistor to external dc voltage. A 1K pull up resistor is a good valve. Leaving the Pin floating, or grounded will disable the unit. To guarantee turn-on, the enable voltage must be above 1.25 V. To disable the unit, the enable voltage must be pulled below 0.7 V. V_{CC} should not be higher than 5 V.

VR_READY - Pin 14
The VRM11.1 modules have a power good indicator output. The output uses positive logic and is open collector. Use 4.7 K resistor to pull Pin 14 to a maximum 5 V. VR_READY is pulled low before starting up or after starting up when there is a fault condition (no output) due to OCP or OVP operating conditions.

Pin Functions (cont'd)

VR_HOT - Pin 15
VR_HOT is an open collector output. Pull this Pin up to 5 V with 4.7 K resistor. This Pin sends an advanced thermal event warning by turning its output to low. This occurs in case the module inductor's core temperature goes above 102 °C. The Pin can be connected to CPU PROC_HOT signal to allow the microprocessor to reduce its power consumption in case of VRM11.1 over temperature running condition.

V_{OUT} - Pin 17, 18, 21, 22, 23, 26, 27
The VRM11.1 has some ceramic output capacitors internally. However, it is necessary to use the following capacitors connected between V_{OUT} and GND.

Output Capacitors		
6 x 470 µF	EEFSE0D471R	2 V, 5mohm, POSCAP
16 x 47 µF		Cer, 0805, X5R
37 x 22 µF		Cer, 0805, X5R

Using these capacitors will result in low output voltage ripple and excellent response to load transient in the system board. It is equally important to use good design practices when configuring the dc distribution system. Low resistance and low inductance PCB layout traces should be utilized, particularly in the high current output section. Remember that the capacitance of the distribution system and the associated ESR are within the feedback loop of the power capabilities, thus affecting the stability and dynamic response of the module.

The output capacitance is an integral part of VRM11.1 design. It effects the load line impedance and load transient response. The VRM11.1 controls the load impedance to the required value from dc up to the feedback loop bandwidth frequency. From the feedback loop frequency, up to 2Mhz, the load line impedance is controlled by the impedance of the bulk capacitor, ceramic, and the PCB power traces. Higher than 2 Mhz, the output load impedance is controlled by the LGA 1366 microprocessor socket power traces and the ceramic capacitors. It is highly recommended to place the ceramic capacitors inside the microprocessor socket cavity and close to it. Place the bulk capacitors close to the VRM11.1 output.

V_{IN} - Pin 30 and Pin 31
The operating input voltage range is 10.2 - 13.8 V. Although the module has some ceramic capacitors (internally); in order to achieve optimum steady state and load transient response, use the following capacitors connected between V_{IN} and GND, as close as possible to the VRM11.1 VIN Pins 30 and 31.

Input Capacitors	
2 x 270 µF	AL, RAD, 20%, 16 V

Optional Horizontal Mount - Pin 32 and 33
Optional horizontal mounting is available upon customer request.

Pin Assignment (Vertical and Horizontal)

Pin Assignments							
Pin	**Function**						
1	VID0	9	Remote Sense(+)	17	Vout	25	GND
2	VID1	10	Remote Sense(-)	18	Vout	26	Vout
3	VID2	11	IMON	19	GND	27	Vout
4	VID3	12	PSI#	20	GND	28	GND
5	VID4	13	OUTEN	21	Vout	29	GND
6	VID5	14	VR_READY	22	Vout	30	Vin
7	VID6	15	VR_HOT	23	Vout	31	Vin
8	VID7	16	GND	24	GND	32 & 33	Horiz. Mechanical Pins

Pin Assignments Card Edge

Pin Assignments							
Pin	**Function**						
1	VIN-	15	VO+	29	VO+	43	VRM_pres#1
2	VIN-	16	VO-	30	VO+	44	VRM_pres#0
3	VIN-	17	VO-	31	VO-	45	PSI
4	VID4	18	VO-	32	VO-	46	VID7
5	VID2	19	VO+	33	VO-	47	VR_hot#
6	VID0	20	VO+	34	VO+	48	VO_SEN-
7	VO_SEN+	21	VO+	35	VO+	49	VID5
8	VR_Ready	22	VO-	36	VO+	50	VID1
9	OUTEN	23	VO-	37	VO+	51	VID3
10	IMON	24	VO-	38	VO+	52	VIN+
11	VID6	25	VO+	39	VO-	53	VIN+
12	VRM_pres#2	26	VO+	40	VO+	54	VIN+
13	VO+	27	VO+	41	VO+		
14	VO+	28	VO+	42	VO+		

Use Tyco part number 1651929-1 or Elcon part number 283-0172-02303 for system connector.

Electrical Specifications

Parameter	Test Conditions	Min	Typ	Max	Units
Absolute Maximums					
Operating Ambient Temperature		0	25	70	°C
Non-Operating Ambient Temperature		-40	25	125	°C
Input Specifications					
Input Voltage	VRM11-1-130-VJ	10.2	12	13.8	Vdc
Input Voltage	VRM11-1-130-XX1J/XX2J	6.5	12	13.8	Vdc
Input Current (No Load)	Enabled		500		mA
Input Current (quiescent)	Converter disabled		10		mA
Input Capacitance (Internal)	Internal to converter		160		uF
Input Capacitance (External)	Recommend customer added capacitance		2 x 270		uF
Output Specifications					
Ouput Voltage		0.5		1.6	V
Output Setpoint Accuracy		-0.1		+0.1	%
Output Regulation (Line)		-2		+2	mV
Output Load Impedence			0.8		mohm
Output Current (continuous)		0		110	A
Output Current (short circuit)		120		150	A
Output Capacitance (Internal)			88		uF
Output Capacitance (External)			6x 470		uF
			16 x 47		mV
			32 x 22		%
Output Ripple/Noise (Peak/Peak)			10		mV
Efficiency	1.5 V, 60 A		89.76		%
	1.2 V, 60 A		88.27		%
	1.1 V, 70 A		87.56		%
Dynamic Load Response (Peak Deviation)	12 V_{in}, 0.5-1.6 V_{out}, 0-100% load at 300 A/us		Per Intel		mV
Dynamic Load Response (Setting Time)	12 V_{in}, 0.5-1.6 V_{out}, 0-100% load at 300 A/us		Per Intel		us

Electrical Specifications (cont'd)

Parameter	Test Conditions	Min	Typ	Max	Units
Turn On Specifications					
Soft Start			2.4		ms
Enable Specifications					
Signal Low (Unit Off)		0		0.87	V
Signal High (Unit On)	12 V_{in}	1.25	3.3	5	V
Protection Specifications					
Over Current Protection	Hiccup Mode		1.23 I_{PEAK}		A
Input Under Voltage (Turn-On)	(VJ / V1J & V2J)		10.1/6.4		V
Input Under Voltage (Turn-Off)	(VJ / V1J & V2J)		9.2/5.6		V
General Specifications					
MTBF	Telcorida SR-332		TBD		Hours
Weight			40		g
Switching Frequency	Per Phase		320		kHz
Material Ratings					
Flammability			UL94V-0		
Material Type			FR4 PCB		

On Bench Test Results

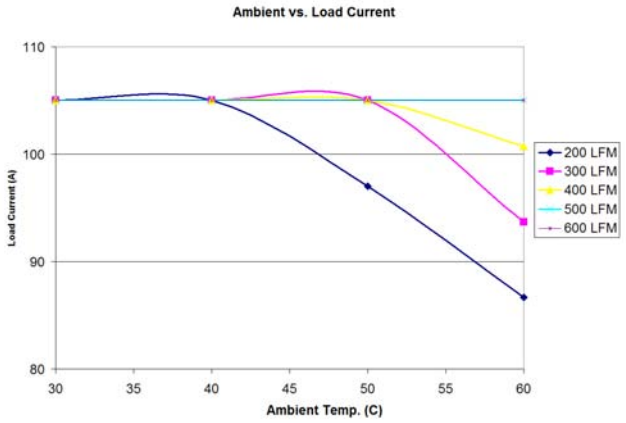


Figure 3a: Thermal Derating Curve (VJ)

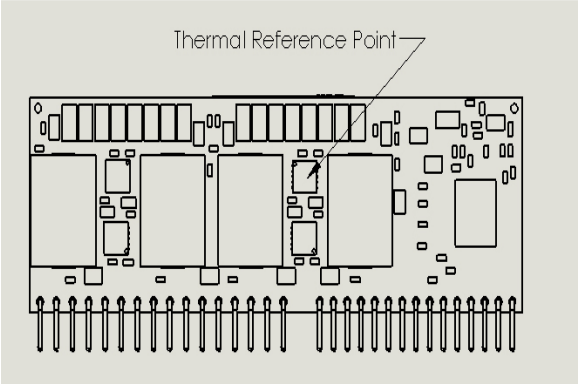


Figure 3b: Thermal Hotspot

In order to simplify the thermal design, a thermal derating plot is provided in figure 3a. However, the thermal performance is heavily dependent on the final system application, therefore the user needs to ensure the thermal reference point show in figure 3b, does not exceed 110 °C. It is recommended that the reference point is measured with a thermal couple or IR camera.

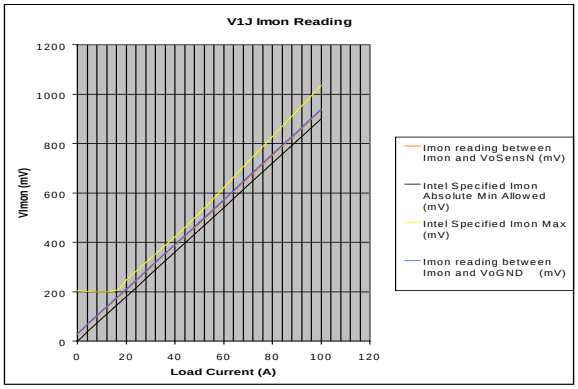


Figure 4: V1J I_{MON} Reading

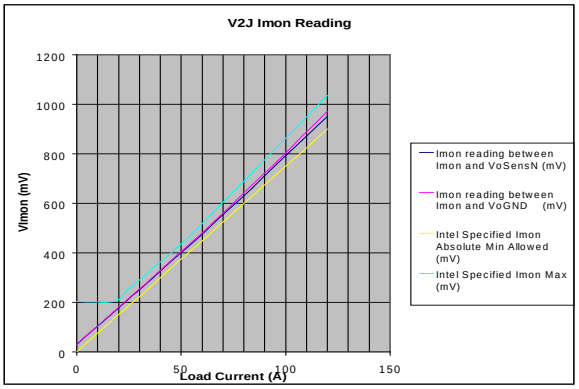


Figure 5: V2J I_{MON} Reading

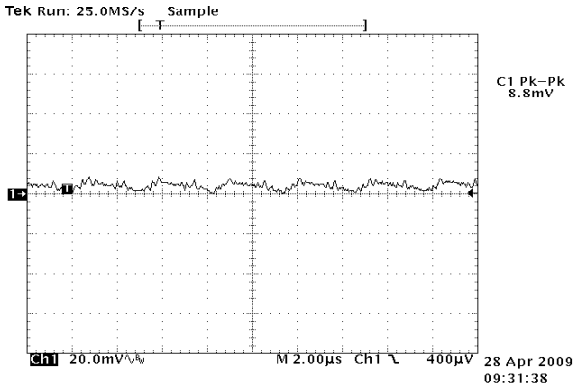


Figure 6: Output Voltage Ripple, V_{OUT}=1.1V, I_{OUT}=20A w/ Phase Dropping Set to 1

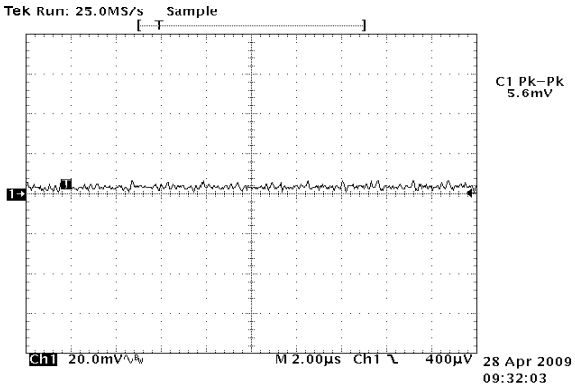


Figure 7: Output Voltage Ripple, V_{OUT}=1.1V, I_{OUT}=20A without Phase Dropping

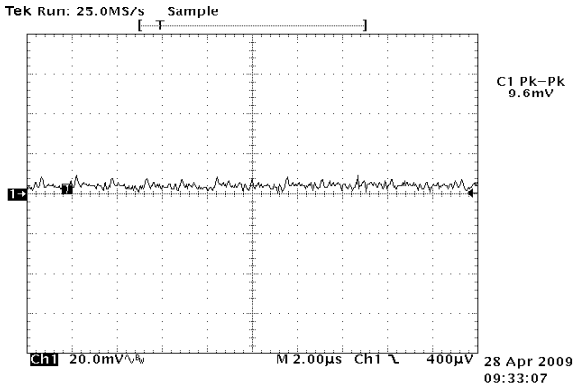


Figure 8: Output Voltage Ripple, V_{OUT}=1.1V, I_{OUT}=85A

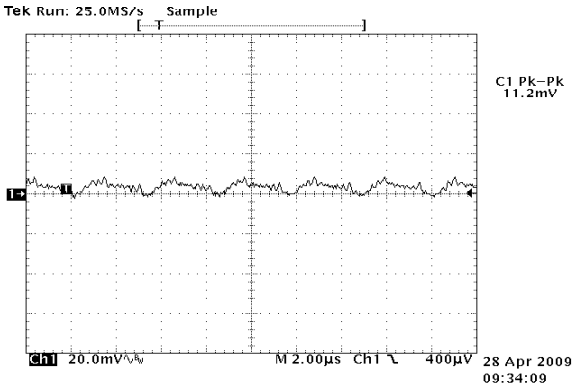


Figure 9: Output Voltage Ripple, V_{OUT}=1.5V, I_{OUT}=20A with Phase Dropping Set to 1

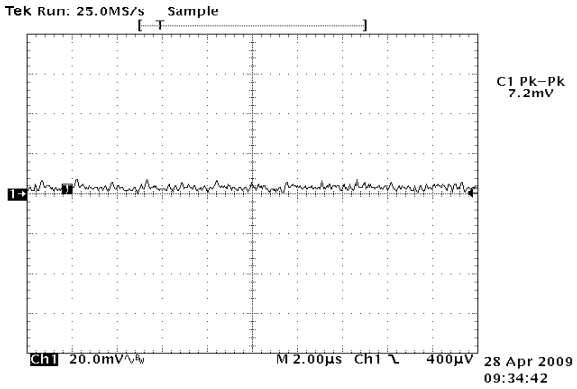


Figure 10: Output Voltage Ripple, V_{OUT}=1.5V, I_{OUT}=20A without Phase Dropping

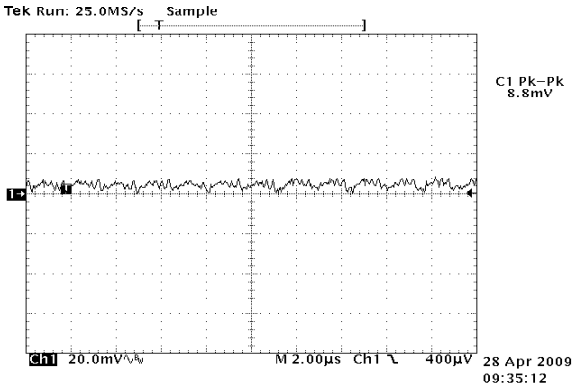


Figure 11: Output Voltage Ripple, V_{OUT}=1.5V, I_{OUT}=85A

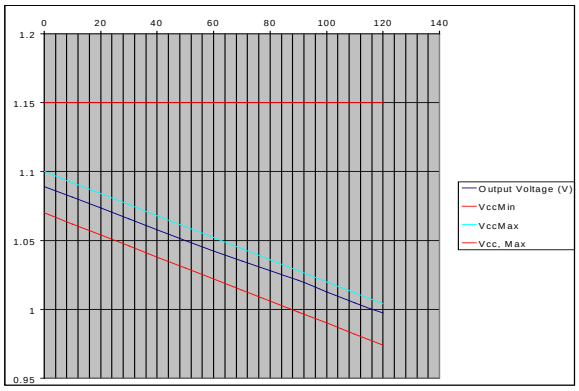


Figure 12: Voltage Droop Measurement
V_{OUT}=1.1V

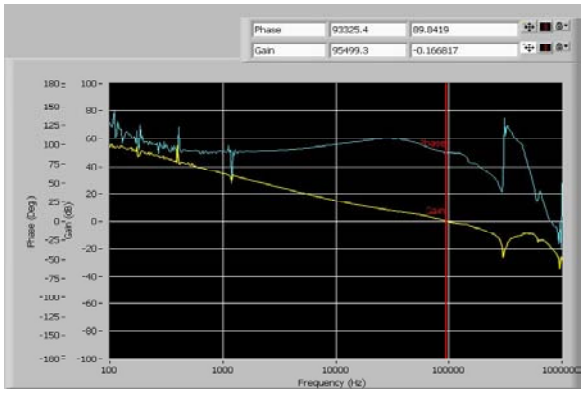


Figure13: Feedback Loop Gain and Phase Margin
V_{OUT}=1.1V, I_{OUT}=0A

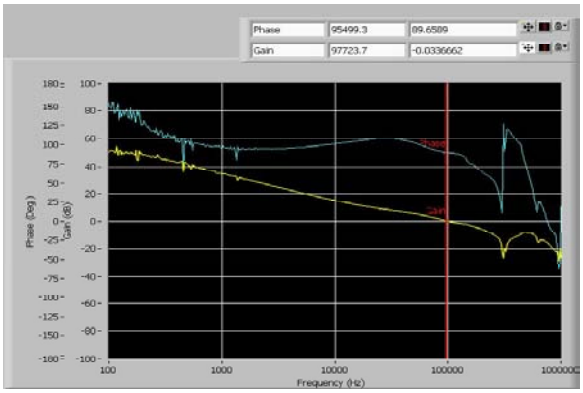


Figure 14: Feedback Loop Gain and Phase Margin
V_{OUT}=1.1V, I_{OUT}=40A

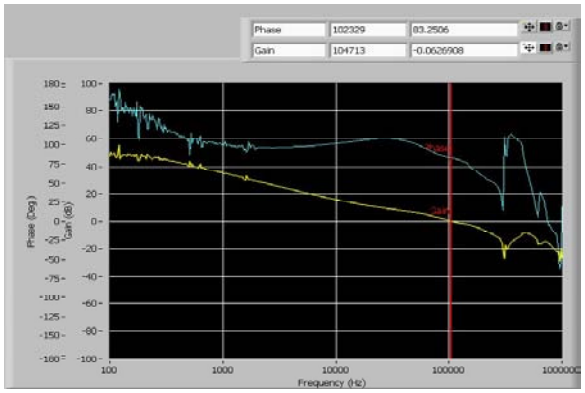


Figure 15: Feedback Loop Gain and Phase Margin
V_{OUT}=1.1V, I_{OUT}=85A

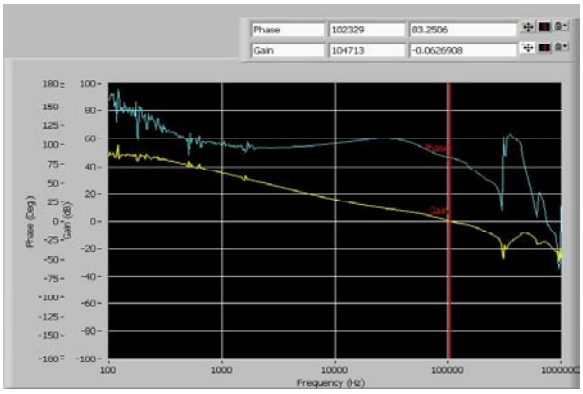


Figure 16: Feedback Loop Gain and Phase Margin
V_{OUT}=1.5V, Iout=0A

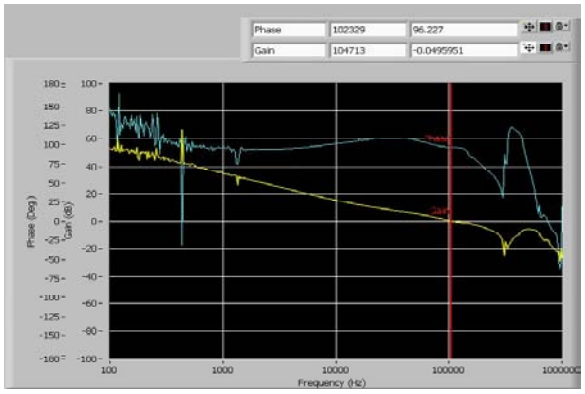


Figure 17: Feedback Loop Gain and Phase Margin
V_{OUT}=1.5V, I_{OUT}=40A

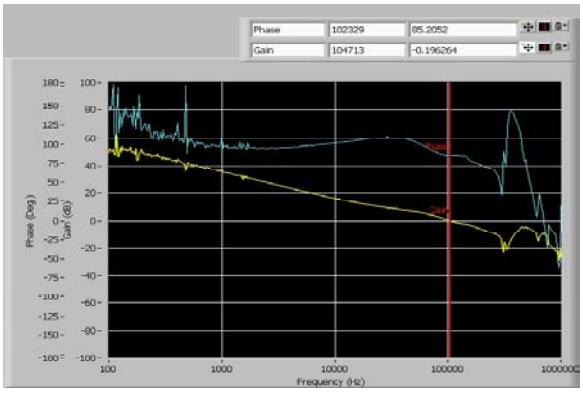


Figure 18: Feedback Loop Gain and Phase Margin
V_{OUT}=1.5V, I_{OUT}=85A

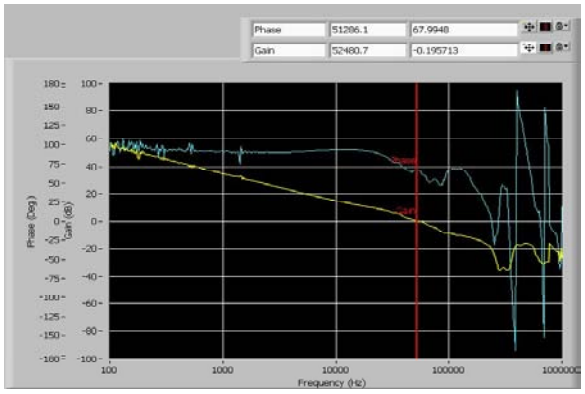


Figure 19: Feedback Loop Gain and Phase Margin,
During PSI asserted mode (drop to one phase)
1.1V, 0A

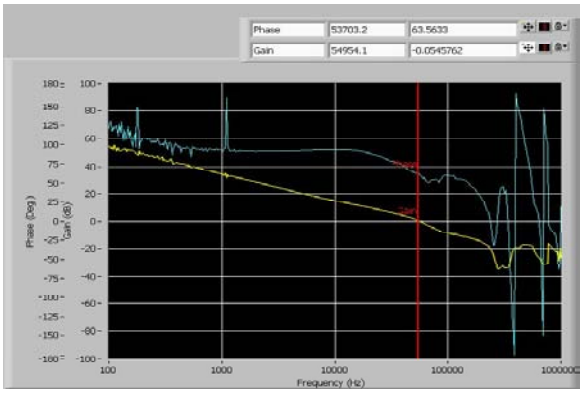


Figure 20: Feedback Loop Gain and Phase Margin
During PSI asserted mode (drop to one phase) 1.1V, 10A

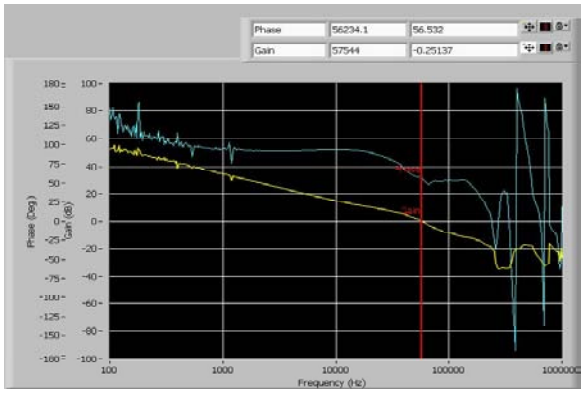


Figure 21: Feedback Loop Gain and Phase Margin
V_{OUT}=1.During PSI asserted mode (drop to one phase)
1.1V, 20A

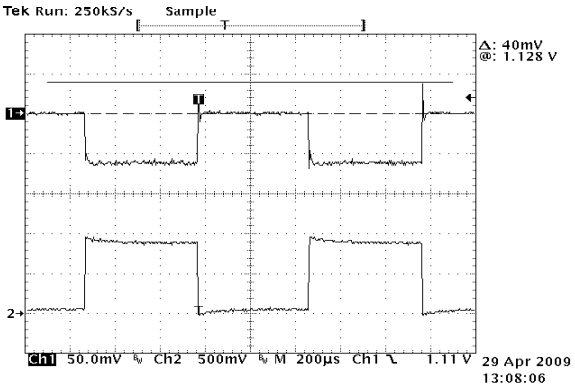


Figure 22: 1.1 V, Transient Response 0 A - 80 A,
Freq = 1KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 200 µs/div

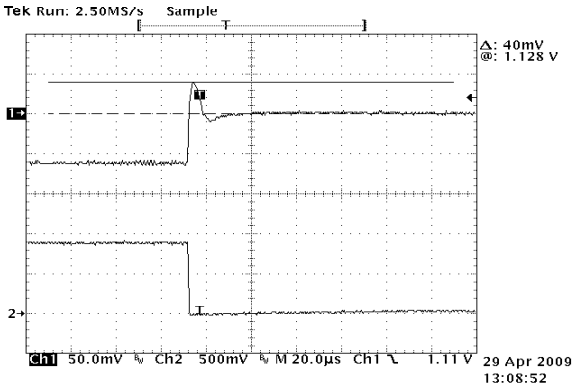


Figure 23: Overshoot, 1.1 V, Transient Response 0 A - 80 A,
Freq = 1KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 20 µs/div

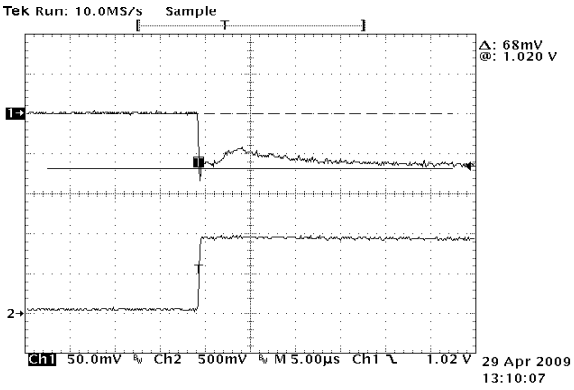


Figure 24: Undershoot, 1.1 V,
Transient Response 0 A - 80 A, Freq = 1 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 5 µs/div

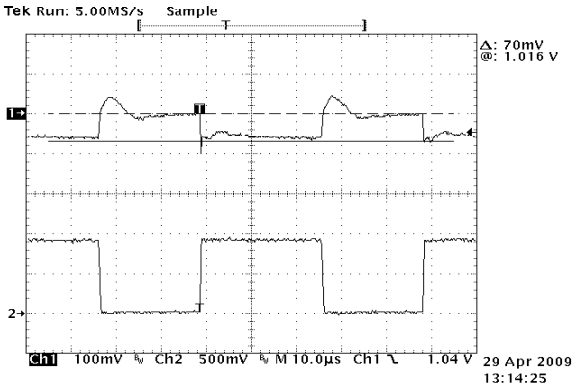


Figure25: 1.1 V, Transient Response 0 A - 80 A, Freq = 20 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 10 µs/div

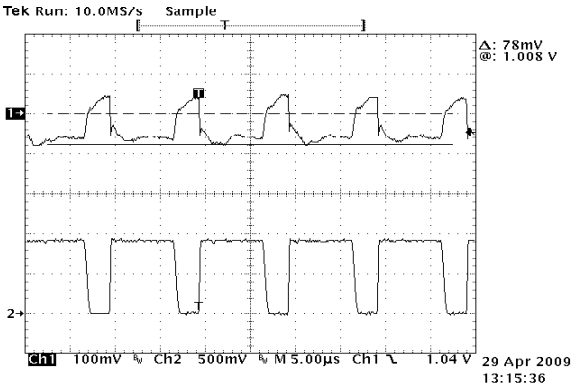


Figure 26: 1.1 V, Transient Response 0 A - 80 A, Freq = 100 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 5 µs/div

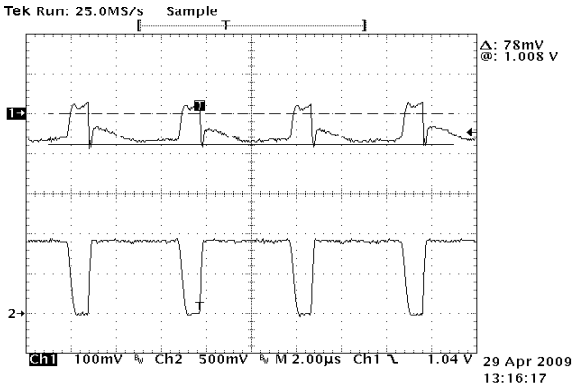


Figure 27: 1.1 V, Transient Response 0 A - 80 A, Freq = 200 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 2 µs/div

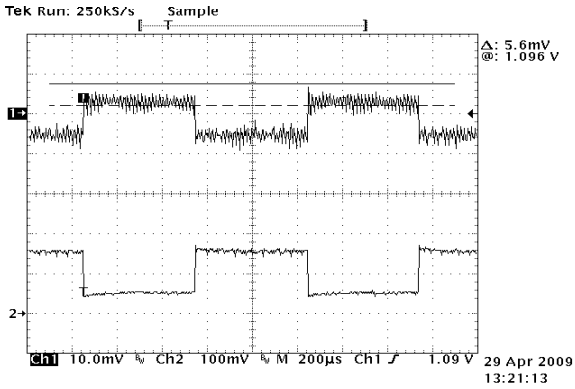


Figure 28: 1.1 V, PSI# Mode,
Transient Response 1 A - 11 A, Freq = 1 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 200 µs/div

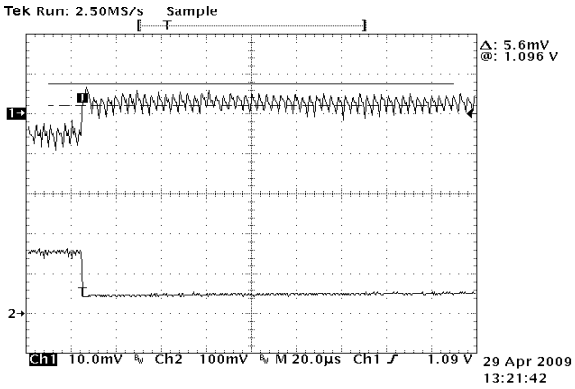


Figure 29: Overshoot, 1.1 V, PSI# Mode,
Transient Response 1 A - 11 A, Freq = 1 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 20 µs/div

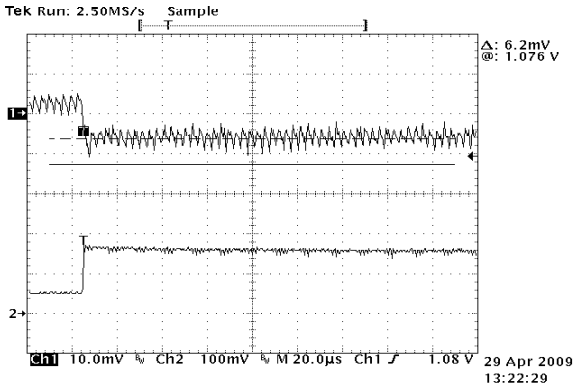


Figure 30: Undershoot, 1.1 V, PSI# Mode,
Transient Response 1 A - 11 A, Freq = 1 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 20 µs/div

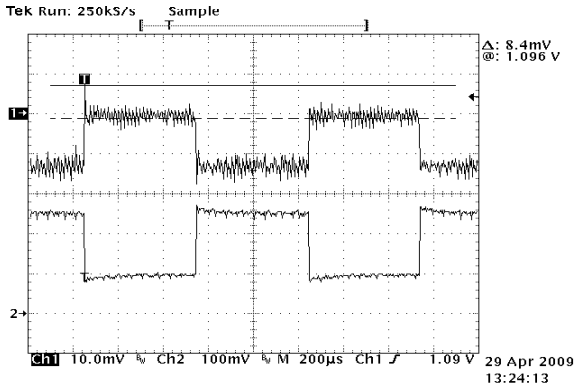


Figure 31: 1.1 V, PSI# Mode,
Transient Response 5 A - 20 A, Freq = 1 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 200 µs/div

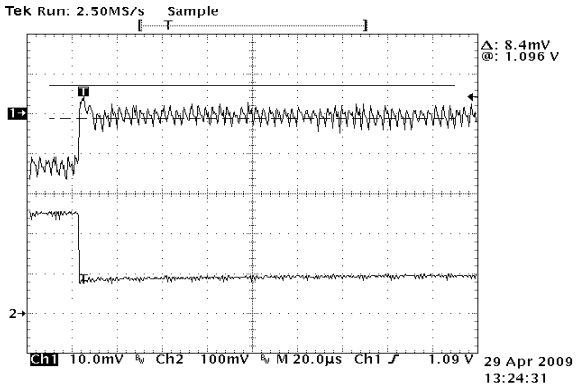


Figure 32: Overshoot, 1.1 V, PSI# Mode,
Transient Response 5 A - 20 A, Freq = 1 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 20 µs/div

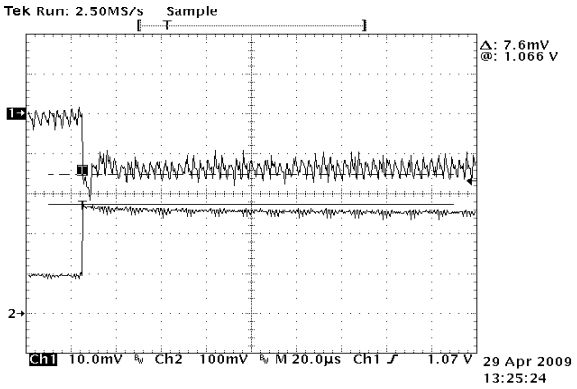


Figure 33: Undershoot, 1.1 V, PSI# Mode,
Transient Response 5 A - 20 A, Freq = 1 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 20 µs/div

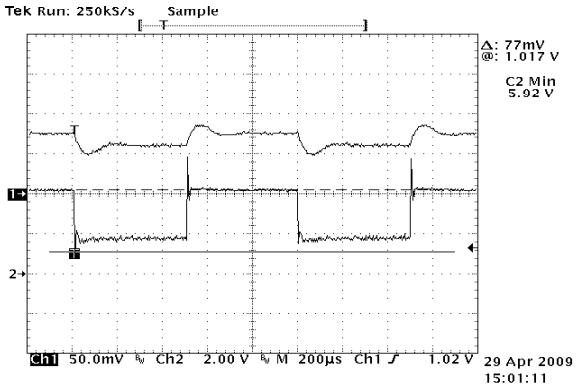


Figure 34: 1.1 V, PSI# Mode,
Transient Response at V_{IN} = 6 V, Freq = 1 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 200 µs/div

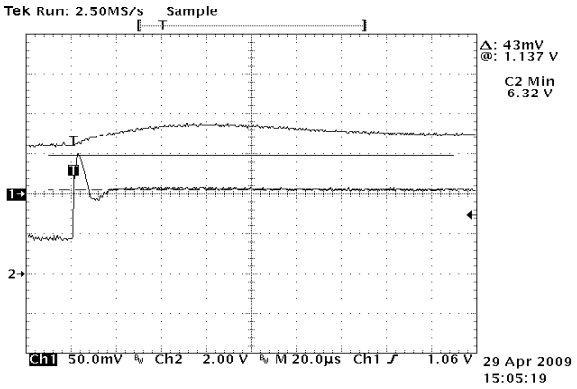


Figure 35: Overshoot, 1.1 V, PSI# Mode,
Transient Response at V_{IN} = 6 V, Freq = 1 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 20 µs/div

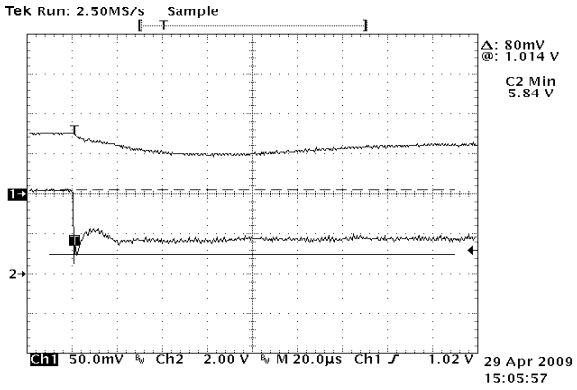


Figure 36: Undershoot, 1.1 V, PSI# Mode, Transient Response at V_{IN} = 6 V, Freq = 1 KHz
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 300 A/µs) 20 µs/div

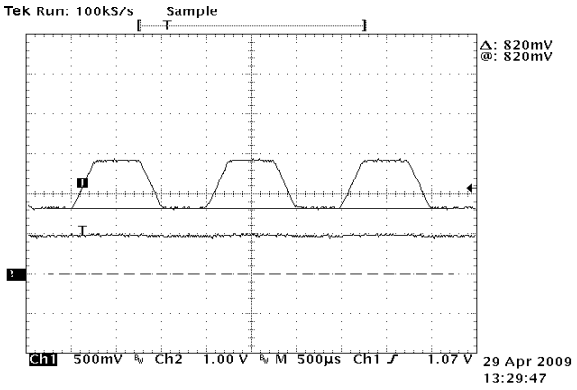


Figure37: Dynamic VID, Static Current Load, Vin=12V
V_{OUTMIN}=0.9V, V_{OUTMAX}=1.5V, I_{OUT}=100A,
(CH1: Output Voltage, CH2: Load current)

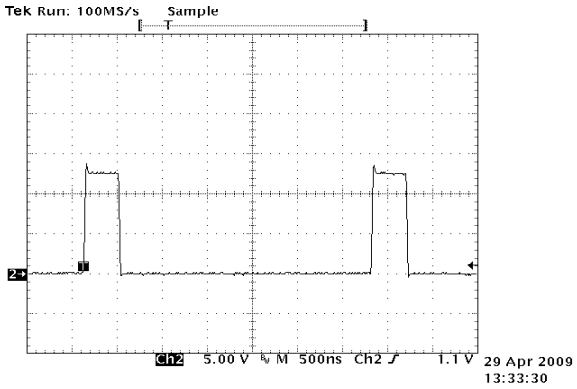


Figure 38: Phase Node Jittering Measurement
V_{IN} = 12V, V_{OUT} set to 1.1V I_{OUT}=0 A,
(CH1: Phase Node Voltage) 600 ns/div

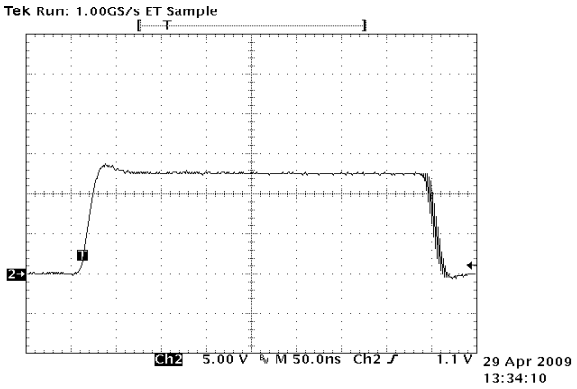


Figure 39: Phase Node Jittering Measurement
V_{IN} = 12V, V_{OUT} set to 1.1V I_{OUT}=0 A,
(CH1: Phase Node Voltage) 50 ns/div

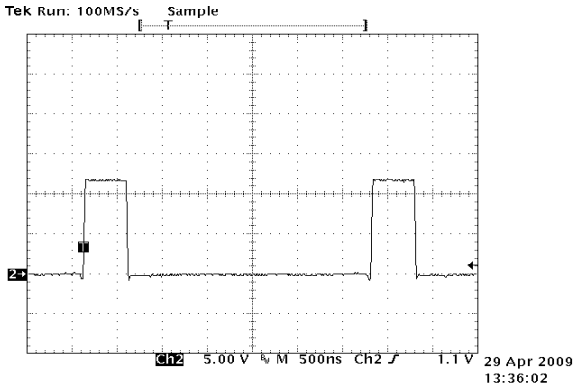


Figure 40: Phase Node Jittering Measurement
V_{IN} = 12V, V_{OUT} set to 1.1V I_{OUT}=85 A,
(CH1: Phase Node Voltage) 600 ns/div

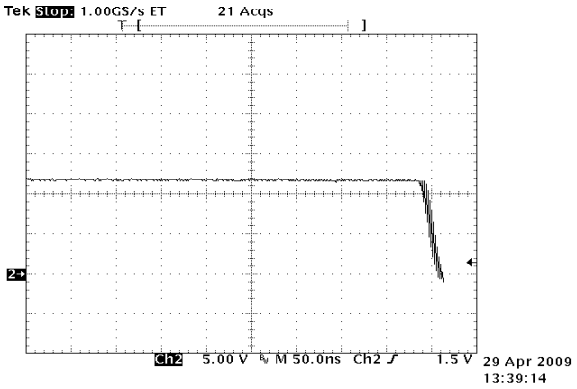


Figure 41: Phase Node Jittering Measurement
V_{IN} = 12V, V_{OUT} set to 1.1V I_{OUT}=85 A,
(CH1: Phase Node Voltage) 50 ns/div

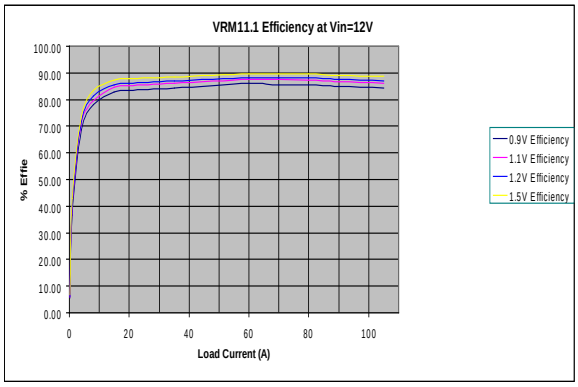


Figure 42: Efficiency
V_{IN}=12V, V_{OUT} is Set @ 0.9, 1.1, 1.2, 1.5V

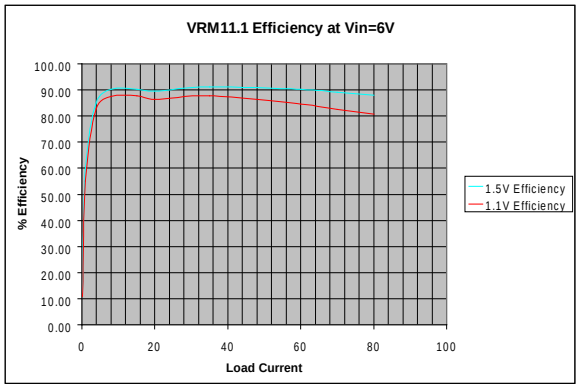
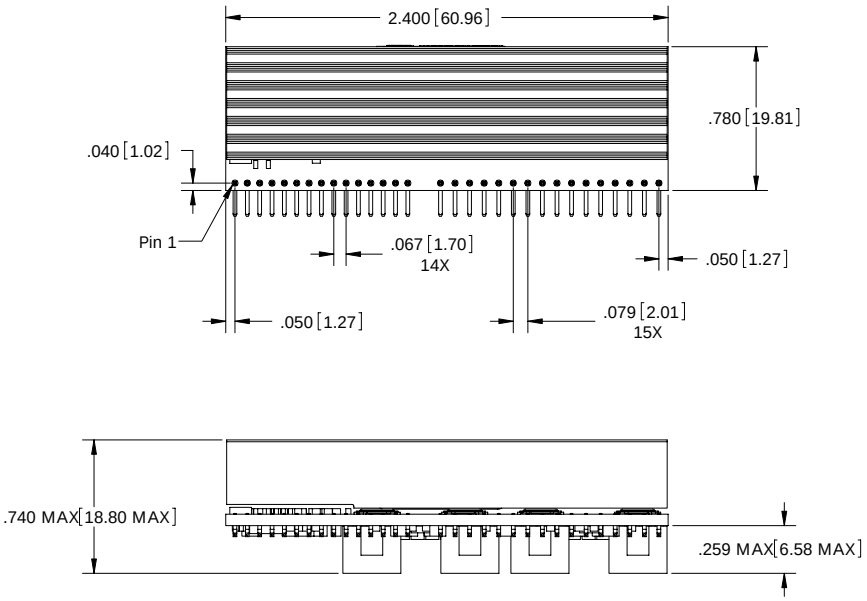


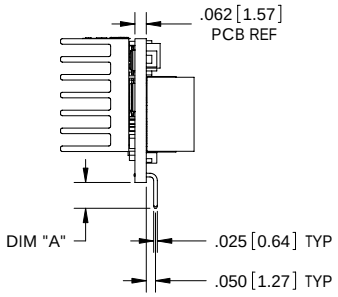
Figure 43: Efficiency
V_{IN} = 6V, V_{OUT} is Set @ V_{OUT} is Set @ 1.1 and 1.5V

Mechanical Drawings

Vertical Through-Hole VRM11-1-130-VJ and VRM11-1-130-V3J

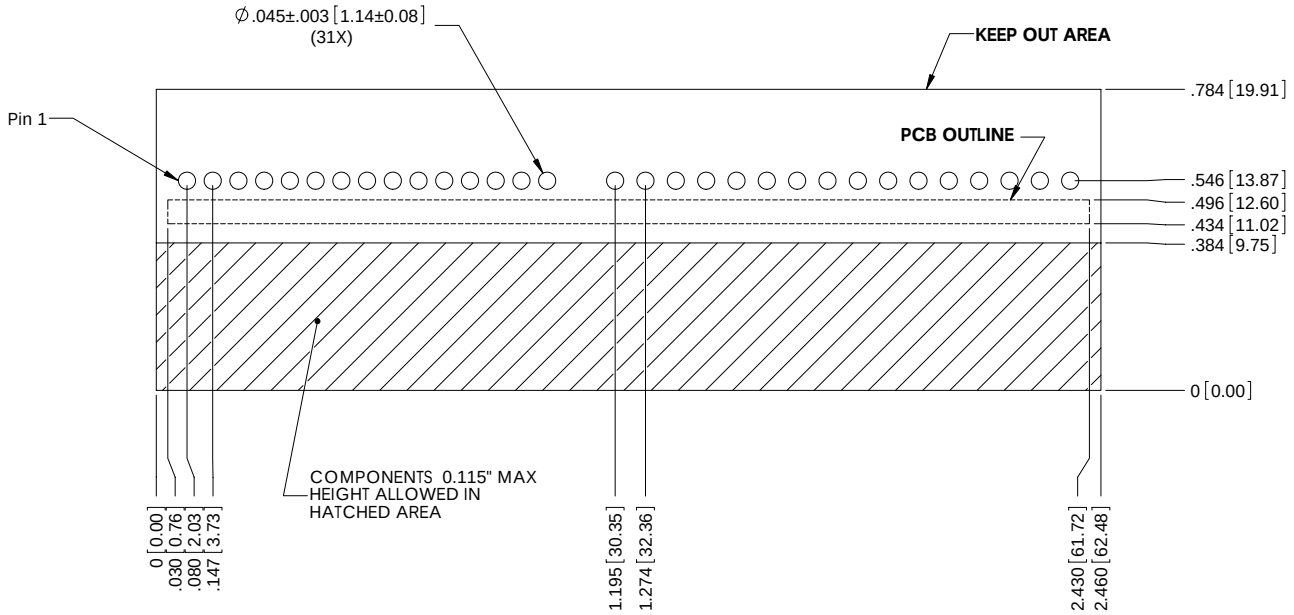
Connecting pins use 100% matte tin (Sn) plating with a nickel (Ni) barrier and are Pb-free. Plating is minimum 200 micro-inches of 100% tin (Sn) over minimum 50 micro-inches of nickel (Ni).





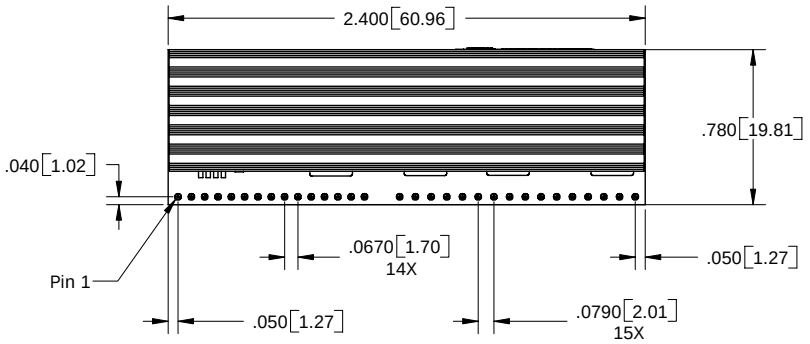
P/N	DIM "A"
VJ	.150"
V3J	.120"

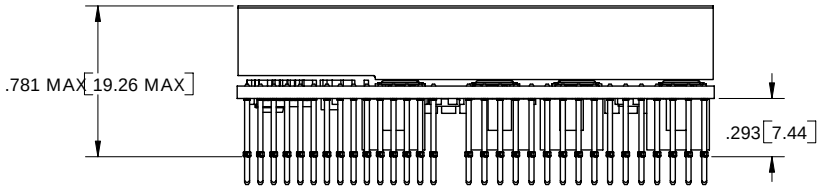
Footprint

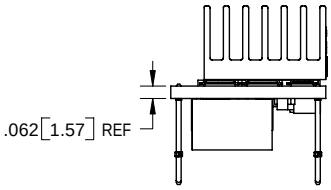


Mechanical Drawings

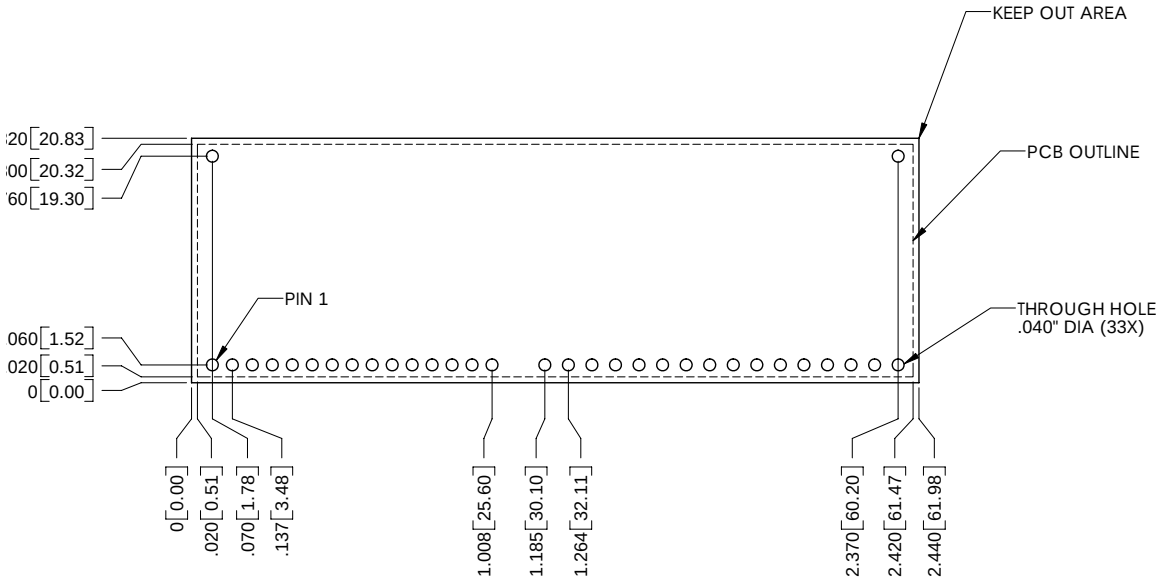
Vertical Through-Hole VRM-11-1-130-HJ







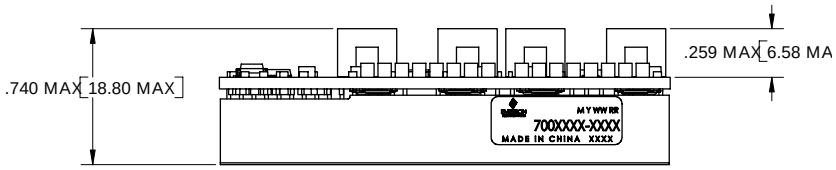
Footprint

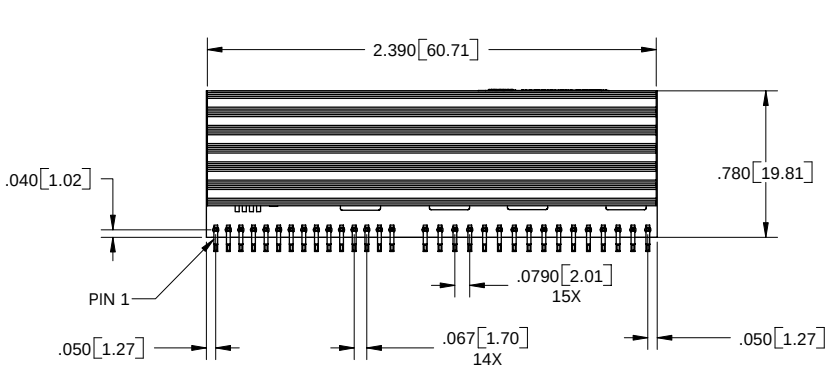


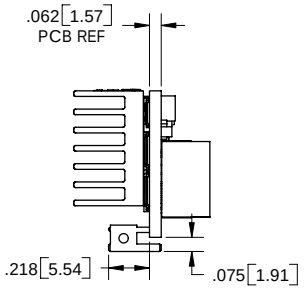
Tolerance Note: ±.015 [0.381]

Mechanical Drawings

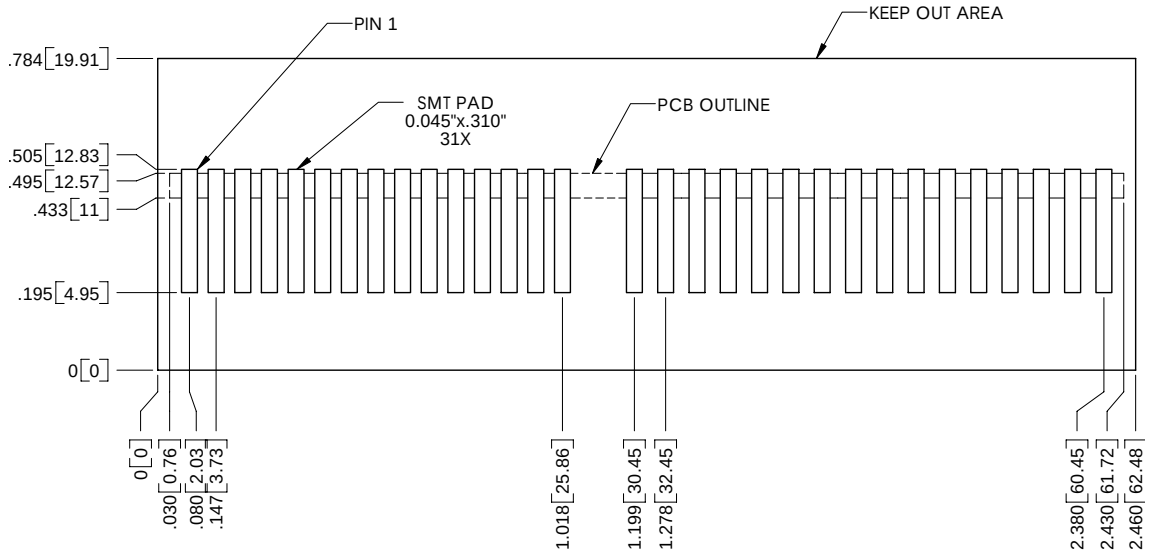
Vertical Surface Mount VRM11-1-130-VSJ







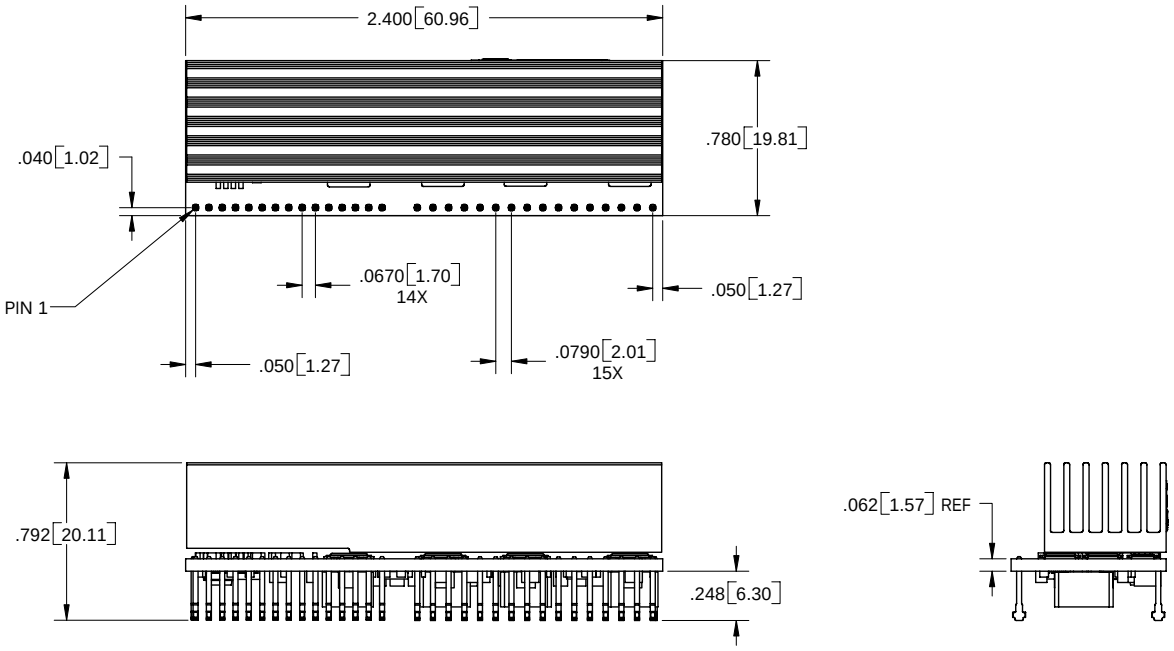
Footprint



Tolerance Note: ±.015 [0.381]

Mechanical Drawings (cont'd)

Horizontal Surface Mount VRM11-1-130-HSJ



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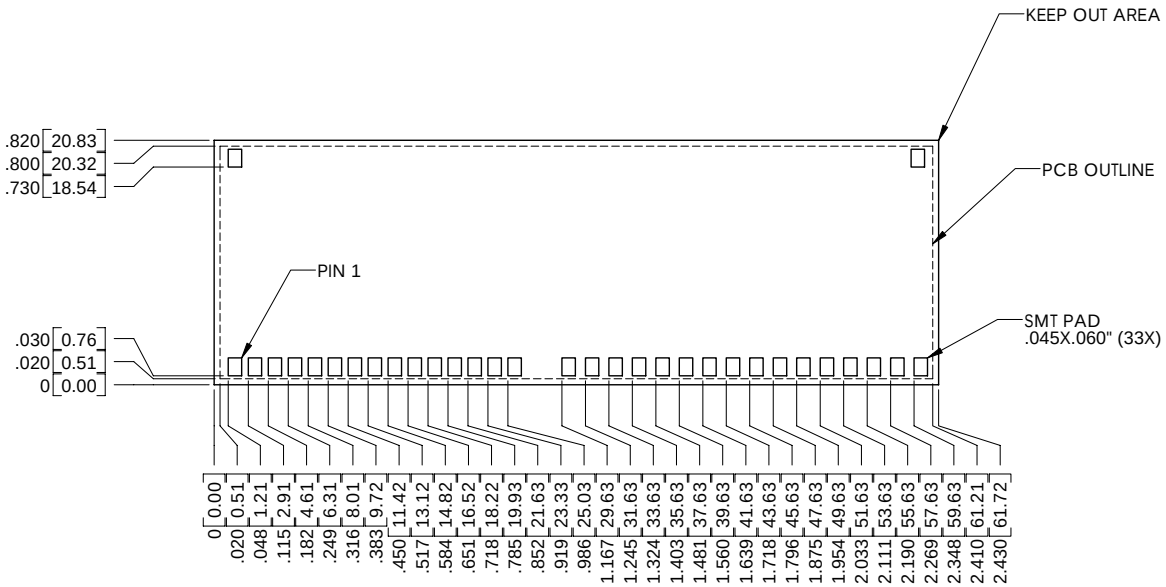
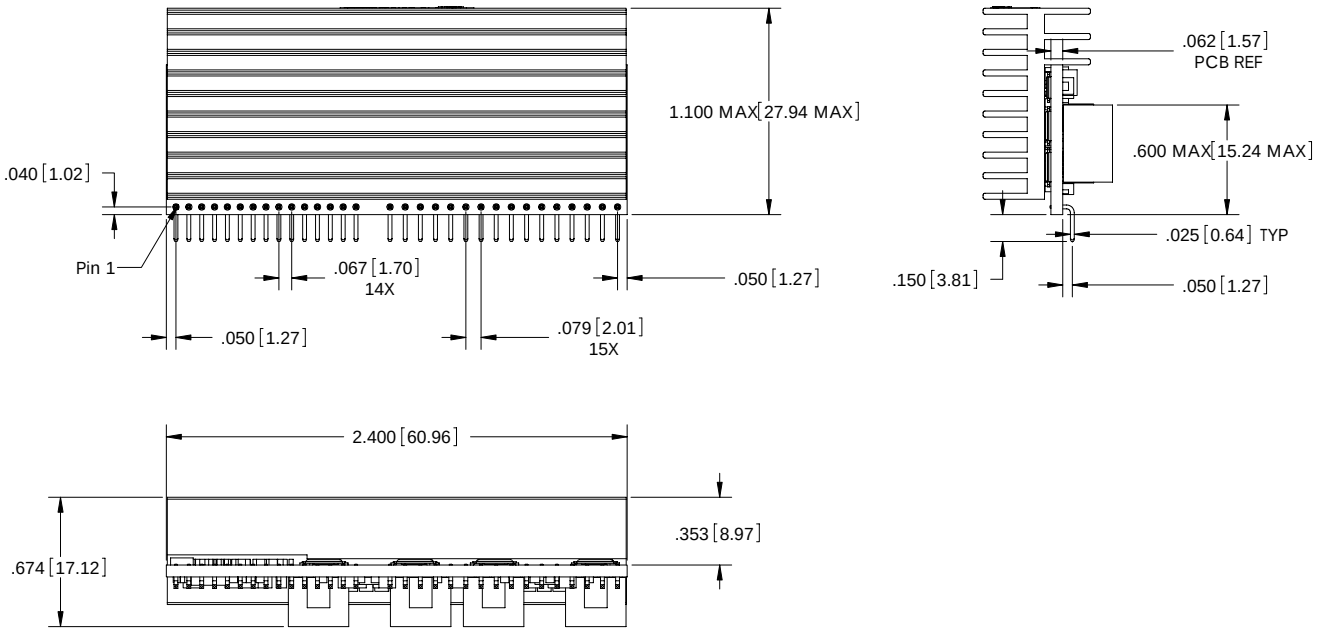


Tolerance Note: 0.015 [0.381]

Mechanical Drawings

Vertical Through-Hole VRM-11-1-130-V1J, VRM-11-1-130-V2J



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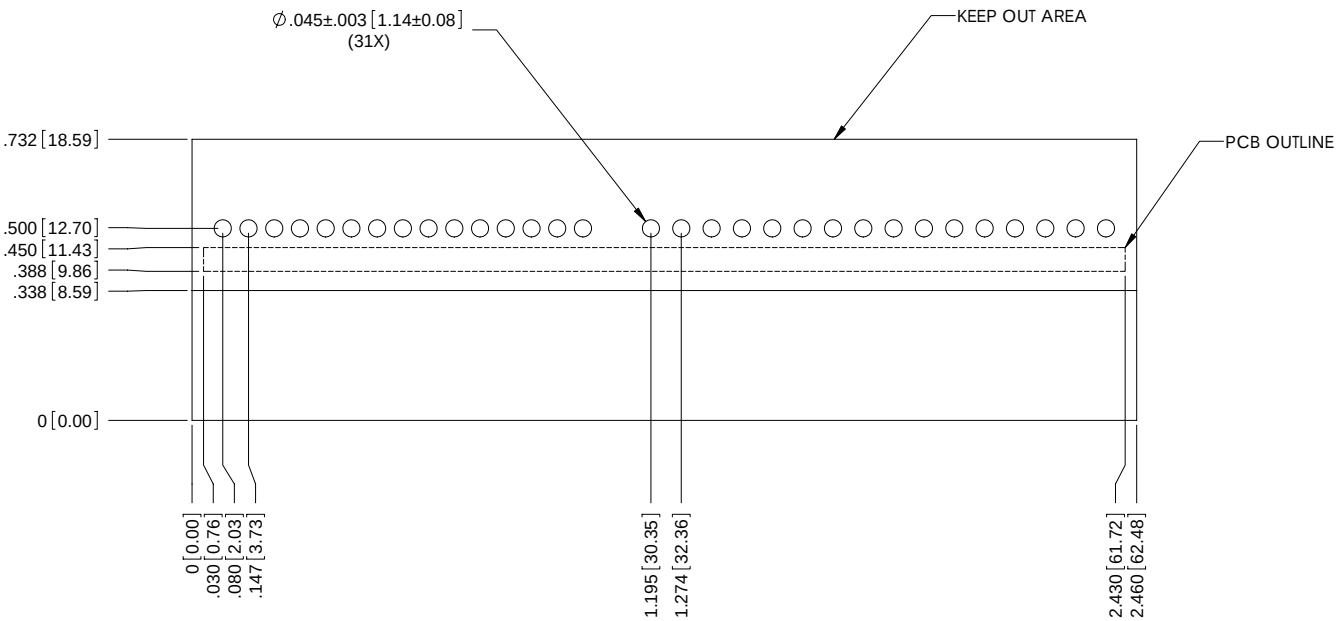
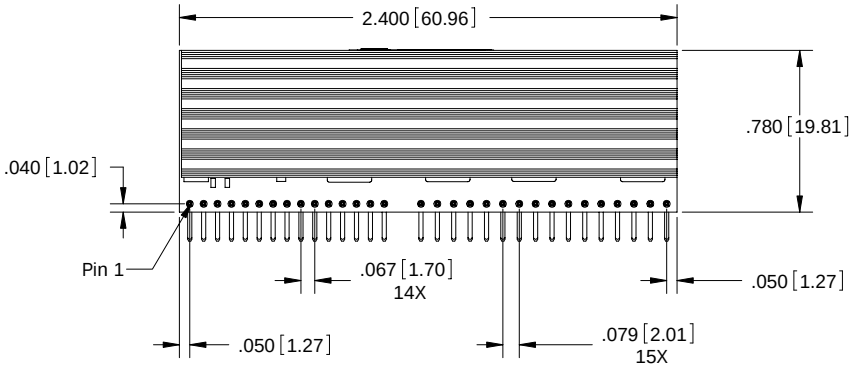


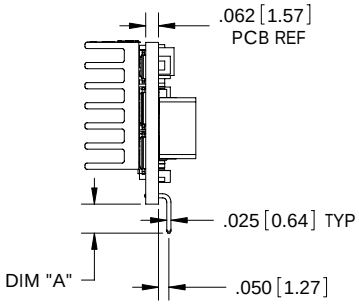
Tolerance Note: 0.015 [0.381]

Mechanical Drawings

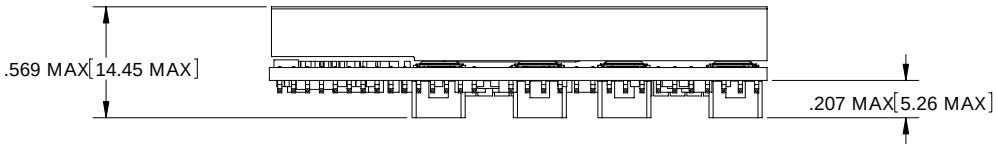
Vertical Through-Hole VRM11-1-130-VAJ and VRM11-1-130-VA3J

Connecting pins use 100% matte tin (Sn) plating with a nickel (Ni) barrier and are Pb-free. Plating is minimum 200 micro-inches of 100% tin (Sn) over minimum 50 micro-inches of nickel (Ni).





P/N	DIM "A"
VJ	.150"
VA3J	.120"



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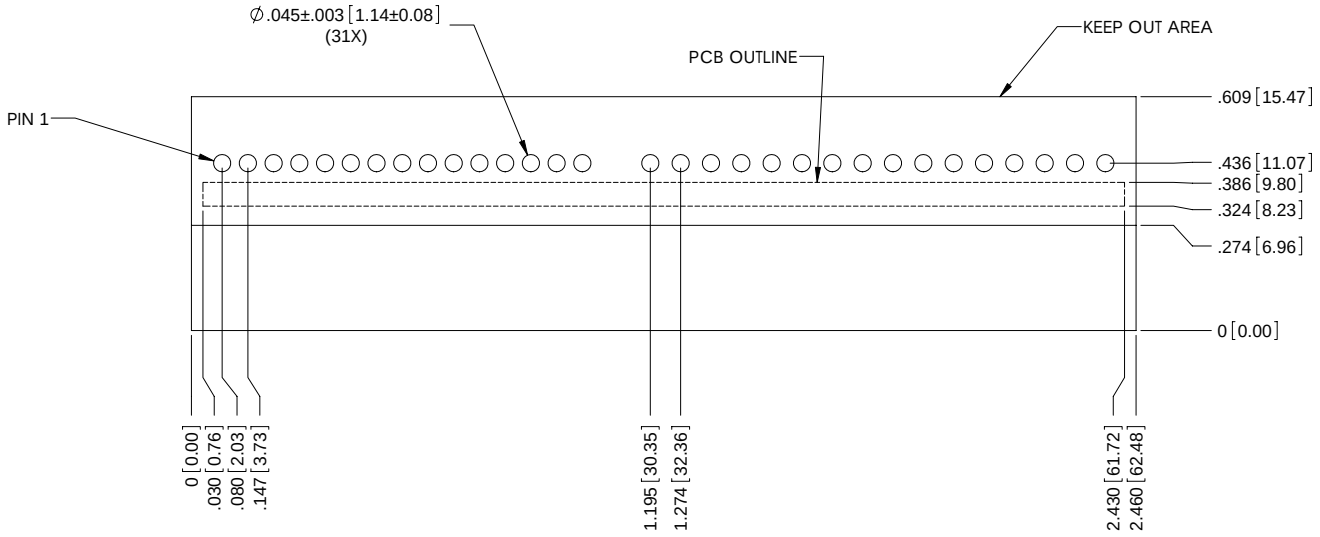
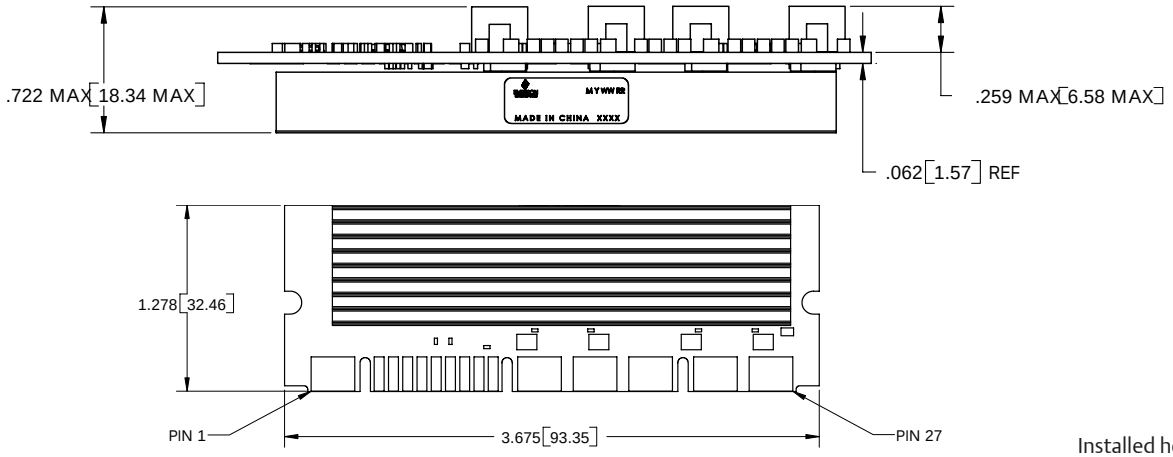


Tolerance Note: 0.015 [0.381]

Mechanical Drawings (cont'd)

Card Edge VRM-11-1-130-CEJ



Installed height is 1.517: (38.5mm)
Tolerance Note: ±0.015 [0.381]

Ordering Information

Output Power (Max.)	Input Voltage (Vdc)	Output Voltage (Vdc)	Output Current (Nominal)	Output Current (Peak)	Peak Efficiency	Pin Length	Load Impedence (mohm)	Model Number
170 W	10.20 - 13.80	0.5 - 1.6	105 A*	140 A	88% at 1.2 Vout	.150	0.8	VRM11-1-130-VJ***
170 W	10.20 - 13.80	0.5 - 1.6	105 A*	140 A	88% at 1.2 Vout	.120	0.8	VRM11-1-130-V3J
112 W	6.00 - 13.80	0.5 - 1.6	70 A**	100 A	88% at 1.2 Vout	.150	0.8	VRM11-1-130-V1J
136 W	6.00 - 13.80	0.5 - 1.6	85 A**	120 A	88% at 1.2 Vout	.150	0.8	VRM11-1-130-V2J
88 W	10.20 - 13.80	0.5 - 1.6	55 A	70 A	87% at 1.5 Vout	.150	1.4	VRM11-1-130-VAJ
88 W	10.20 - 13.80	0.5 - 1.6	55 A	70 A	87% at 1.5 Vout	.120	1.4	VRM11-1-130-VA3J
175 W	10.20 - 13.80	0.5 -1.6	110 A	140 A	87% at 1.5 Vout	NA	0.8	VRM11-1-130-CEJ

* 600 LFM at 45 °C ambient temperature. **300 LFM at 50 °C ambient temperature. ***Other mounting options available.

Model Number System with Options

Product Family	Industry Standard		Rated Output Current		Mounting Option	Options	RoHS Compliance
VRM	**11-1**	**-**	**130**	**-**	**XX**	**X**	**J**
Product Family VRM = Voltage Regulated Module	**Industry Standard** 11-1 = 11.1		**Rated Output Current** 130 = 70-140 Amp		**Mounting Option** H = Horizontal THT V = Vertical THT CE = Card Edge HS = Horizontal SMT VS = Vertical SMT	**Options** Blank = 0.8mohm load impedance 1 = Positive Logic and wide input voltage, 100 A 2 = Positive Logic and wide input voltage, 120 A A = 1.4mohm load impedance, 70 A 3 = 0.8mohm load impedance, .120 pin A3 = 1.4mohm load impedance, 70 A, .120 pin	**RoHS Compliance** J = Pb free (RoHS 6/6 compliant)

Technical Reference Note

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